ATS9625

250MS/s 16-Bit PCI Express Digitizer with user-programmable FPGA

- User programmable Coprocessor FPGA
- 2 channels sampled at 16-bit resolution
- 250 MS/s real-time sampling rate
- 75 dB Signal To Noise Ratio
- PCI Express (8-lane) interface
- 2 GigaSample on-board dual-port memory
- Continuous streaming mode
- Asynchronous DMA device driver
- AlazarDSO oscilloscope software
- Software Development Kit supports C/C++, C#, MATLAB and LabVIEW
- Linux driver available

RoHS compliant 2002/95/EC

Product	Bus	Operating System	Channels	Sampling Rate	Bandwidth	Memory Per Channel	Resolution
ATS9625	PCIe x8	Win XP/Vista/7, Linux 2.6+ 32bit/64 bit	2	250 MS/s to 50 MS/s	1 ~ 150 MHz	Up to 2 GigaSample	16 bits

Overview

ATS9625 is an 8-lane PCI Express (PCIe x8), dual-channel, high speed, 16 bit, 250 MS/s waveform digitizer card with an on-board, user-programmable FPGA, called a Coprocessor FPGA.

The Coprocessor FPGA is an Altera Stratix III device with on-chip memory, hardware multipliers, DSP blocks and a fast fabric that allows both integer based and floating point digital signal processing.

All data acquired by the on-board A/D converters flows through the Coprocessor FPGA, allowing user-defined FPGA circuit to process the data in real time and at hardware speed.

The main difference between ATS9626 and ATS9625 is input coupling: ATS9626 provides dc coupling, whereas ATS9625 provides ac coupling.

ATS9625 is supplied with AlazarDSO software that lets the user get started immediately without having to go through a software development process.

Users who want to design their own Coprocessor FPGA must purchase ATS962x Coprocessor FPGA Development Kit (also called ATS962x-FDK).

Users who need to integrate the ATS9625 in their own program can purchase a software development kit, ATS-SDK for C/C++ and VB, or ATS-VI for LabVIEW for Windows or a Linux based ATS-Linux for C/C++ and LabVIEW for Linux.

All of this advanced functionality is packaged in a low power, half-length PCI Express card.

Applications

Optical Coherence Tomography (OCT)

Radar/RF Signal Recording & Analysis

Ultrasonic & Eddy Current NDT/NDE

Terabyte Storage Oscilloscope

High Resolution Oscilloscope

Lidar

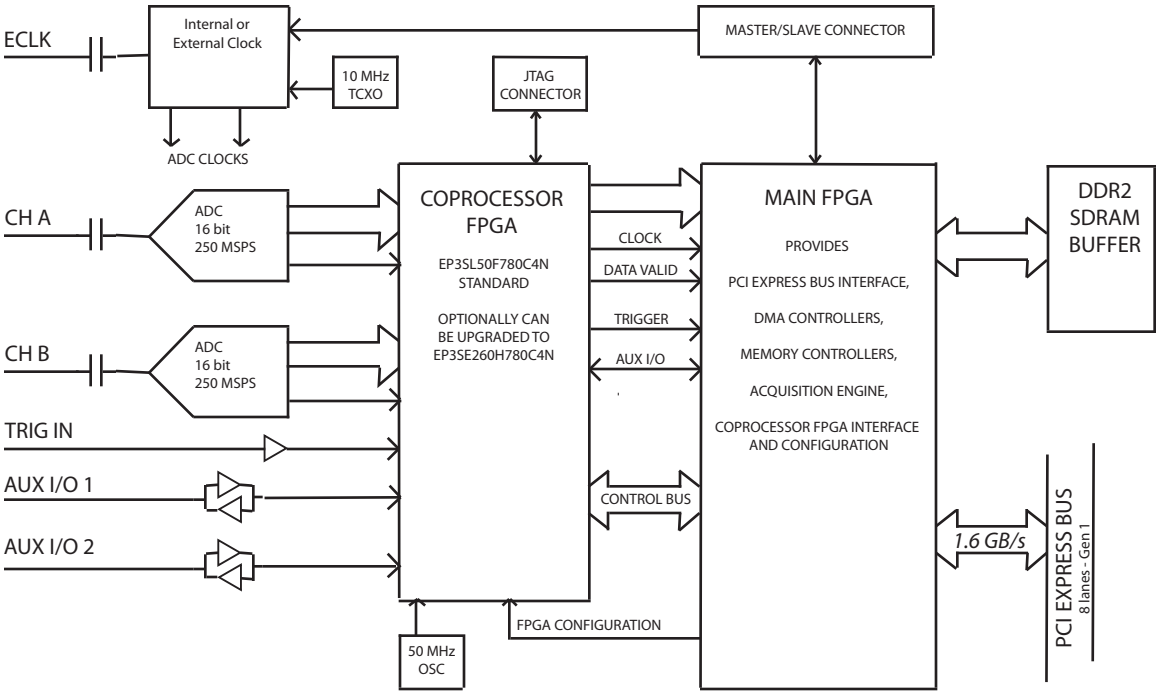
Spectroscopy

Digital Down Conversion (DDC)

Multi-Channel Transient Recording

ATS9625

250MS/s 16-Bit PCI Express Digitizer with user-programmable FPGA



PCI Express Bus Interface

ATS9625 interfaces to the host computer using an 8-lane PCI Express bus. Each lane operates at 2.5 Gbps.

According to PCIe specification, an 8-lane board can be plugged into any 8-lane or 16-lane slot, but not into a 4-lane or 1-lane slot. As such, ATS9625 requires at least one free 8-lane or 16-lane slot on the motherboard.

The physical and logical PCIe x8 interface is provided by an on-board FPGA, which also integrates acquisition control functions, memory management functions and interface to Coprocessor FPGA. This very high degree of integration maximizes product reliability.

AlazarTech's bus benchmark has been proven on many computers, including workstation and server class machines from Dell and HP, as well as no-name machines built around motherboards from Intel, ASUS, Tyan, Supermicro etc.

Users must always be wary of throughput specifications from manufacturers of waveform digitizers. Some unscrupulous manufacturers tend to specify the raw, burst-mode throughput of the bus. Others mention data throughput rates to operating system kernel memory, not user accessible memory.

AlazarTech, on the other hand, specifies the benchmarked sustained throughput to buffers in user space.

To achieve such high throughput, a great deal of proprietary memory management logic and kernel mode drivers have been designed by AlazarTech.

Analog Input

An ATS9625 has two transformer coupled analog input channels. Each channel has analog input bandwidth from 1 MHz to 150 MHz.

The full scale input range is fixed at 2.5 V_{p-p} calibrated at 10 MHz input signal.

Input impedance of both channels is fixed at 50Ω. It must be noted that this impedance is dynamic in nature and not resistive.

Acquisition System

ATS9625 PCI Express digitizers use state of the art 250 MSPS, 16-bit ADCs to digitize the input signals. The real-time sampling rate of the ADCs ranges from 250 MS/s down to 50 MS/s.

The two channels are guaranteed to be simultaneous, with a maximum clock skew of 10 ps. Additive jitter of the clock distributor circuit is less than 225 fs_{rms}.

An acquisition can consist of multiple records, with each record being captured as a result of one trigger event. A record can contain both pre-trigger and post-trigger data.

Infinite number of triggers can be captured by ATS9625, when it is operating using dual-port memory.

In between the multiple triggers being captured, the acquisition system is re-armed by the hardware within 256 sampling clock cycles.

This mode of capture, sometimes referred to as Multiple Record, is very useful for capturing data in appli-

cations with a very rapid or unpredictable trigger rate. Examples of such applications include medical imaging, ultrasonic testing, OCT and NMR spectroscopy.

Coprocessor FPGA

ADC data flows through the Coprocessor FPGA before it is stored in the on-board memory or transferred to host PC memory.

Programming the Coprocessor FPGA involves a design flow that revolves around Quartus II software from Altera Corporation. An FPGA programmer can use VHDL or Verilog or even schematic-based design entry and then compile the design, a process that generates a downloadable FPGA binary file.

ModelSim simulator can be used to do functional simulation to verify the design.

Alternately, the FPGA can be designed in MATLAB Simulink environment and DSP Builder software from Altera can be used to bring the design into Quartus II, where compilation can take place.

It should be noted that the ATS962x-FDK (ATS962x Coprocessor FPGA Development Kit) offered by AlazarTech (and sold separately) offers example projects in VHDL source code only.

Downloading a new FPGA binary file into the Coprocessor FPGA is very quick and easy. The download process takes approximately 125 milliseconds for the standard Coprocessor FPGA.

By pre-processing the ADC data in the Coprocessor FPGA, users can customize the entire personality of the ATS9625.

Some examples of Coprocessor FPGAs are: decimating filter for protection against anti-aliasing; digital receivers using a programmable NCO; Optical Coherence Tomography signal processing using FFTs; autocorrelation circuit for lidar applications; hardware averaging for spectroscopy applications ...

Optional High Capacity Coprocessor FPGA

The standard Coprocessor FPGA is an Altera Stratix III EP3SL50F780C4N device. For some users, this FPGA may not have enough resources to implement their entire design.

In such situations, it is possible to order the ATS9625 with a Coprocessor Upgrade to EP3SE260H780C4N FPGA.

Note that orders for high capacity FPGA may have a significant lead-time.

On-Board Acquisition Memory

ATS9625 features an on-board dual-ported memory buffers of 2 Gigasamples.

Acquisition memory can either be divided equally between the two input channels or devoted entirely to one of the channels.

The main advantage of having on-board memory is that it acts as a very deep FIFO between the Analog to Digital converters and PCI Express bus, allowing very fast sustained data transfers across the bus, even if the operating system or another motherboard resource temporarily interrupts DMA transfers.

Maximum Sustained Transfer Rate

PCI Express support on different motherboards is not always the same, resulting in significantly different sustained data transfer rates. The reasons behind these differences are complex and varied and will not be discussed here.

ATS9625 users can quickly determine the maximum sustained transfer rate for their motherboard by inserting their card in a PCIe slot and running the Tools:Benchmark:Bus tool provided in AlazarDSO software.

ATS9625, which is equipped with dual-port on-board memory, will be able to achieve this maximum sustained transfer rate.

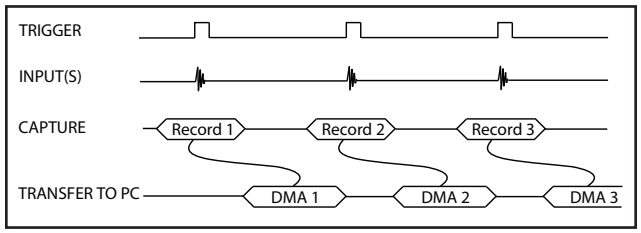
Recommended Motherboards

Many different types of motherboards have been benchmarked by AlazarTech. The best performance is provided by motherboards that use the Intel x58 chipset and iCore 7 processors. The motherboard that has consistently given the best throughput results (as high as 1.7 GB/s) has been the ASUS P6T7 and the new P9X79 Pro.

Older motherboards, such as Intel S5000PSLSATA that use the S5000 chipset have also provided very good throughput.

Traditional AutoDMA

In order to acquire both pre-trigger and post-trigger data in a dual-ported memory environment, users can use Traditional AutoDMA.



Data is returned to the user in buffers, where each buffer can contain from 1 to 8191 records (triggers). This number is called RecordsPerBuffer.

Users can also specify that each record should come with its own header that contains a 40-bit trigger timestamp.

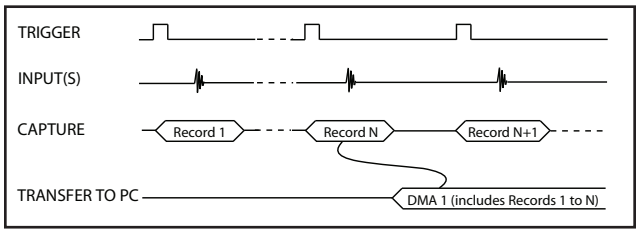
A BUFFER_OVERFLOW flag is asserted if more than 512 buffers have been acquired by the acquisition system, but not transferred to host PC memory by the AutoDMA engine.

In other words, a BUFFER_OVERFLOW can occur if more than 512 triggers occur in very rapid succession, even if all the on-board memory has not been used up.

No Pre-Trigger (NPT) AutoDMA

Many ultrasonic scanning and medical imaging applications do not need any pre-trigger data: only post-trigger data is sufficient.

NPT AutoDMA is designed specifically for these applications. By only storing post-trigger data, the memory bandwidth is optimized and the entire on-board memory acts like a very deep FIFO.



Note that a DMA is not started until RecordsPerBuffer number of records (triggers) have been acquired and written to the on-board memory.

NPT AutoDMA buffers do not include headers, so it is not possible to get trigger time-stamps.

More importantly, a BUFFER_OVERFLOW flag is asserted only if the entire on-board memory is used up. This provides a very substantial improvement over Traditional AutoDMA.

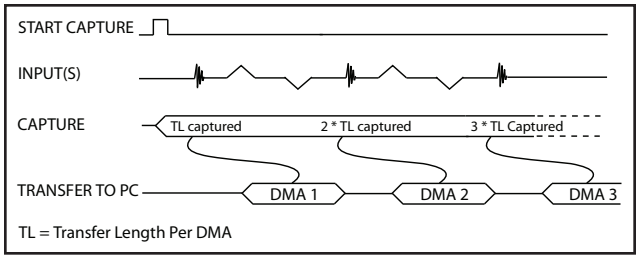
NPT AutoDMA can easily acquire data to PC host memory at the maximum sustained transfer rate of the motherboard without causing an overflow.

This is the recommended mode of operation for most ultrasonic scanning, OCT and medical imaging applications.

Continuous AutoDMA

Continuous AutoDMA is also known as the data streaming mode.

In this mode, data starts streaming across the PCI bus as soon as the ATS9625 is armed for acquisition. It is important to note that triggering is disabled in this mode.



Continuous AutoDMA buffers do not include headers, so it is not possible to get trigger time-stamps.

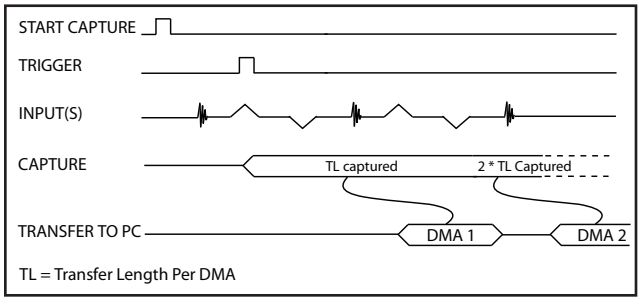
A BUFFER_OVERFLOW flag is asserted only if the entire on-board memory is used up.

The amount of data to be captured is controlled by counting the number of buffers acquired. Acquisition is stopped by an AbortCapture command.

Continuous AutoDMA can easily acquire data to PC host memory at the maximum sustained transfer rate of the motherboard without causing an overflow. This is the recommended mode for very long signal recording.

Triggered Streaming AutoDMA

Triggered Streaming AutoDMA is virtually the same as Continuous mode, except the data transfer across the bus is held off until a trigger event has been detected.



Triggered Streaming AutoDMA buffers do not include headers, so it is not possible to get trigger time-stamps.

A BUFFER_OVERFLOW flag is asserted only if the entire on-board memory is used up.

As in Continuous mode, the amount of data to be captured is controlled by counting the number of buffers acquired.

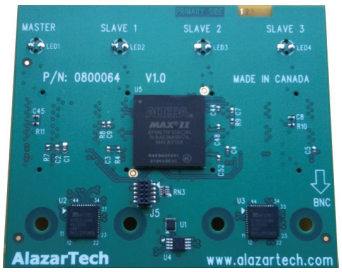
Acquisition is stopped by an AbortCapture command.

Triggered Streaming AutoDMA can easily acquire data to PC host memory at the maximum sustained transfer rate of the motherboard without causing an overflow.

This is the recommended mode for RF signal recording that has to be started at a specific time, e.g. based on a GPS pulse.

Master/Slave Systems

Users can create a multi-board Master/Slave system by synchronizing up to four ATS9625 boards using an appropriate SyncBoard-9625.



SyncBoard-9625 is available as a 2x or a 4x model: the 2x model allows a 2-board Master/Slave system whereas the 4x model allows 2, 3 or 4 board Master/Slave systems.

SyncBoard-9625 is a mezzanine board that connects to the Master/Slave connector along the top edge of the ATS9625 and sits parallel to the motherboard. For additional robustness, users can secure the SyncBoard-9625 to a bracket mounted on each of the ATS9625 boards.

The Master board's clock and trigger signals are copied by the SyncBoard-9625 and supplied to all the Slave boards. This guarantees complete synchronization between the Master board and all Slave boards.

It should be noted that SyncBoard-9625 does not use a PLL-based clock buffer, allowing the use of variable frequency clocks in Master/Slave configuration.

A Master/Slave system samples all inputs simultaneously and also triggers simultaneously on the same clock edge.

Asynchronous DMA Driver

The various AutoDMA schemes discussed above provide hardware support for optimal data transfer. However, a corresponding high performance software mechanism is also required to make sure sustained data transfer can be achieved.

This proprietary software mechanism is called Async DMA (short for Asynchronous DMA).

A number of data buffers are posted by the application software. Once a data buffer is filled, i.e. a DMA has been completed, ATS9625 hardware generates an interrupt, causing an event message to be sent to the application so it can start consuming data. Once the data has been consumed, the application can post the data buffer back on the queue. This can go on indefinitely.

One of the great advantages of Async DMA is that almost 95% of CPU cycles are available for data processing, as all DMA arming is done on an event-driven basis.

To the best of our knowledge, no other supplier of waveform digitizers provides asynchronous software drivers. Their synchronous drivers force the CPU to manage data acquisition, thereby slowing down the overall data acquisition process.

Triggering

ATS9625 is equipped with sophisticated digital triggering options, such as programmable trigger thresholds and slope on any of the input channels or the External Trigger input.

Coprocessor FPGA has access to external trigger and two auxiliary I/O signals and users can create sophisticated custom trigger circuits.

The user can specify the number of records to capture in an acquisition, the length of each record and the amount of pre-trigger data.

A programmable trigger delay can also be set by the user. This is very useful for capturing the signal of interest in a pulse-echo application, such as ultrasound, radar, lidar etc.

Timebase

ATS9625 timebase can be controlled either by on-board low-jitter VCO or by optional External Clock.

On-board low-jitter VCO uses an on-board 10 MHz TCXO as a reference clock.

External Clock

While the ATS9625 features low jitter VCO and a 10 MHz TCXO as the source of the timebase system, there may be occasions when digitizing has to be synchronized to an external clock source.

ATS9625 includes an SMA input for an external clock signal, which can be a sine wave or 1.6V digital signal.

Input impedance for the External Clock input is fixed at 50 Ω. External clock input is always ac-coupled.

There are two types of External Clock supported by ATS9625. These are described below.

Fast External Clock

A new sample is taken by the on-board ADCs for each rising edge of this External Clock signal.

In order to satisfy the clocking requirements of the ADC chips being used, Fast External Clock frequency must always be higher than 50 MHz and lower than 250 MHz.

This is the ideal clocking scheme for OCT applications

10 MHz Reference Clock

It is possible to generate the sampling clock based on an external 10 MHz reference input. This is useful for RF systems that use a common 10 MHz reference clock.

ATS9625 uses an on-board low-jitter VCO to gen-

erate the 250 MHz high frequency clock used by the ADC. This 250 MS/s sampled data can then be decimated by a custom Coprocessor FPGA.

Dummy Clock Switchover

OCT applications require interfacing the ATS9625 to a variable clock frequency (called k-clock) from a swept-source laser.

In most cases, k-clock frequency can be out of specification for a short period of time, i.e. the frequency is slower than 50 MHz for a short period of time.

ATS9625 has a built-in Dummy Clock generator and a clock switchover mechanism that can be used to avoid operating the A/D chips outside of their specifications.

This unique feature of the ATS9625 can be the difference between a fully working OCT system and one that cannot provide reliable data.

AUX Connectors

ATS9625 provides two AUX (Auxiliary) SMA connectors that can be used for interfacing to external digital signals.

When configured as a Trigger Output, AUX BNC connector outputs a 5 Volt TTL signal synchronous to the ATS9625 Trigger signal, allowing users to synchronize their test systems to the ATS9625 Trigger.

When combined with the Trigger Delay feature of the ATS9625, this option is ideal for ultrasonic and other pulse-echo imaging applications.

AUX connector can also be used as a Trigger Enable Input and Clock Output.

Another application for AUX connector is that users can input the 1 PPS pulse from a GPS receiver into the ATS9625 (and the Coprocessor FPGA).

Calibration

Every ATS9625 digitizer is factory calibrated to NIST-traceable standards. To recalibrate an ATS9625, the digitizer must either be shipped back to the factory or a qualified metrology lab.

AlazarDSO Software

ATS9625 is supplied with the powerful AlazarDSO software that allows the user to setup the acquisition hardware and capture, display and archive the signals.

An optional Stream-To-Disk add-on module for AlazarDSO allows users to stream data to hard disk. For the fastest possible streaming, the hard disks have to be used in a RAID 0 configuration.

Users are also able to write their own Plug-In modules. A Plug-In is a DLL that is called each time AlazarDSO receives a data buffer. Many different data processing and control functions can be built into a Plug-In. Examples include Averaging, Co-Adding, controlling acquisition based on an external GPS module etc.

AlazarDSO software also includes powerful tools for benchmarking the computer bus and disk drive.

Software Development Kits

AlazarTech provides easy to use software development kits for customers who want to integrate the ATS9625 into their own software.

A Windows compatible software development kit, ATS-SDK is also offered. It allows programs written in C/C++, C# and MATLAB to fully control the ATS9625. Sample programs are provided as source code.

A set of high performance VIs for LabVIEW, called ATS-VI, can also be purchased.

ATS-Linux

AlazarTech offers ATS9625 binary drivers for CentOS 6.3 x86_64 with kernel 2.6.32-279.5.2.el6.x86_64. These drivers are also 100% compatible with RHEL 6.3.

Also provided is a GUI application called AlazarFrontPanel that allows simple data acquisition and display. AlazarFrontPanel does not support Dual Port Memory.

Source code example programs are also provided, which demonstrate how to acquire data programmatically using a C compiler.

If customers want to use ATS9625 in any Linux distribution other than the one listed above, they must purchase a license for Linux driver source code and compile the driver on the target operating system. A Non-Disclosure Agreement must also be executed between the customer's organization and AlazarTech.

All such source code disclosures are made on an as-is basis with limited support from the factory.

Processing Using Multiple CPU Cores

Programmers can take advatage of multiple cores available in modern CPUs to speed up signal processing.

Benchmarks have shown that a quad-core CPU can perform real-time averaging at a rate of 1.0 GB/s and only use up 20% of CPU cycles. Increasing the number of cores or decreasing the sample rate reduces CPU usage even further.

One of the main applications of using multiple cores to do signal processing is Quantum Computing and Spectroscopy applications, where each record contains partial information about the signal of interest and a large number of records must be accumulated to gather a representative dataset.

GPU Based Signal Processing

Graphical Processing Units (GPUs) are becoming an increasingly popular method of doing fast signal processing.

ATS-GPU allows customers to interface ATS9625 to Open CL 1.0 compatible GPUs.

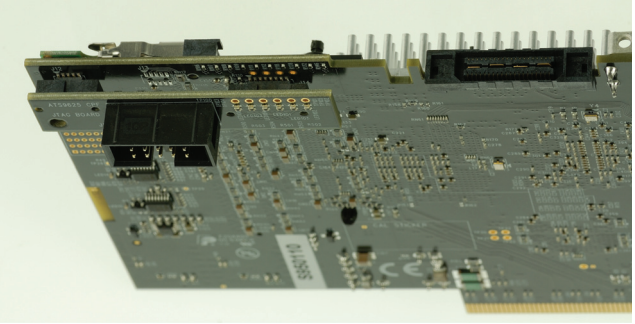
This means that users can do real-time 4096 point FFTs on acquired data in single channel mode for trigger repeat rates up to 100 KHz.

FPGA Development Kit

Customers who want to design their own Coprocessor FPGA must purchase the ATS962x Coprocessor FPGA Development Kit, which is sold separately.

This kit consists of example project provided in VHDL source code and all required project files for Quartus II software.

Also included is a JTAG Debug Board that will allow FPGA designers to debug their designs using SignalTap in-system logic analyzer and USB Blaster cable from Altera.



To further assist the user, AlazarTech will also include a very high quality 1 meter long PCI Express bus extension cable that will allow the ATS9625 to be brought out of the chassis and on to the bench, so various LEDs are visible.

Customers must have good working knowledge of high speed digital design techniques and FPGA development using Altera tools in order to take advantage of the ATS9625 FPGA Development Kit.

AlazarTech will not provide support for FPGA development if it is deemed by AlazarTech support team that the user is not sufficiently conversant with digital design techniques or development tools.

Furthermore, AlazarTech's responsiblity for FPGA Development Kit is limited to providing a fully working example project, VHDL source code, testbench and documentation. All issues relating to custom FPGA fitting and timing closure are the exclusive resposibility of the customer.

ATS9625

250MS/s 16-Bit PCI Express Digitizer with user-programmable FPGA

System Requirements

Personal computer with at least one free x8 or x16 PCI Express (v1.0a, v1.1 or v2.0) slot, 2 GB RAM, 100 MB of free hard disk space, SVGA display adaptor and monitor with at least a 1024 x 768 resolution.

Power Requirements

+12V	2.0 A, typical
+3.3V	2.0 A, typical

Physical

Size	Single slot, half length PCI card (4.2 inches x 6.5 inches)
Weight	250 g

I/O Connectors

ECLK, CH A, CH B, TRIG IN, AUX I/O 1, AUX I/O 2	SMA female connectors

Environmental

Operating temperature	0 to 55 degrees Celcius
Storage temperature	-20 to 70 degrees Celcius
Relative humidity	5 to 95%, non-condensing

Acquisition System

Resolution	16 bits
Bandwidth (-3dB) AC-coupled, 50Ω	1 MHz - 150 MHz
Number of channels	2, simultaneously sampled
Maximum Sample Rate	250 MS/s single shot
Minimum Sample Rate	1 KS/s single shot for internal clocking
Full Scale Input range:	2.5V p-p (calibrated at 10 MHz input)
Input coupling	AC only
Input impedance	50Ω ±1%
Input protection	±4V (DC + peak AC for CH A, CH B and EXT only without external attenuation)

Timebase System

Timebase options	Internal Clock or External Clock (Optional)
Internal Sample Rates	250 MS/s, 125 MS/s,100 MS/s, 50 MS/s, 20 MS/s, 10 MS/s, 5 MS/s, 2 MS/s, 1 MS/s, 500 KS/s, 200 KS/s, 100KS/s, 50 KS/s, 20 KS/s, 10 KS/s, 5 KS/s, 2 KS/s, 1 KS/s
Internal Clock accuracy	±2 ppm

Dynamic Parameters

Typical values measured on CH A of a randomly selected ATS9625. Input signal was provided by a Marconi 2018A signal generator, followed by multi-pole band-pass filters (TTE Q36T family). Inputs were not averaged.

	5 MHz	10 MHz	20 MHz	50 MHz	100 MHz
SNR	75.29 dB	75.02 dB	75.04 dB	74.39 dB	71.67 dB
SINAD	74.47 dB	74.12 dB	74.24 MHz	74.13 dB	70.72 dB
SFDR	91.60 dB	91.03 dB	90.87 dB	86.92 dB	79.95 dB
THD	-82.11 dB	-82.05 dB	-81.99 dB	-85.85 dB	-84.18 dB
ENOB	12.08	12.02	12.04	12.02	11.45

Fast External Clock Input

Connector	ECLK SMA connector
Signal Level	200 mVp-p to 1.6 Vp-p sine wave or square wave
Input impedance	50Ω
Input coupling	AC
Maximum frequency	250 MHz for Fast External Clock
Minimum frequency	50 MHz for Fast External Clock
Sampling Edge	Rising

Dummy Clock Switchover

Switchover mode	Available only when Fast External Clock is selected
Switchover start	Upon end of each record
Switchover time	Programmable with 5 ns resolu-ton

10 MHz Reference Input

Connector	ECLK SMA connector
Signal Level	200 mVp-p to 1.6 Vp-p sine wave or square wave
Input impedance	50Ω
Input Coupling	AC coupled
Input Frequency	10 MHz ± 0.25 MHz
Sampling Clock Freq.	250 MHz

Triggering System

Mode	Edge triggering with hysteresis
Comparator Type	Digital comparators for internal (CH A, CHB) triggering and analog comparators for TRIG IN (External) triggering
Number of Trigger Engines	2
Trigger Engine Combination	OR,
Trigger Engine Source	CH A, CH B, EXT, Software or None, independently software selectable for each of the two Trigger Engines
Hysteresis	±5% of full scale input, typical
Trigger sensitivity	±10% of full scale input range. This implies that the trigger system may not trigger reliably if the input has an amplitude less than ±10% of full scale input range selected

Trigger level accuracy	±5%, typical, of full scale input range of the selected trigger source
Bandwidth	50 MHz
Trigger Delay	Software selectable from 0 to 9,999,999 sampling clock cycles
Trigger Timeout	Software selectable with a 10 us resolution. Maximum settable value is 3,600 seconds. Can also be disabled to wait indefinitely for a trigger event

TRIG IN (External Trigger) Input

Input type	Digital triggering (LVTTL)
Input impedance	3 KΩ
Coupling	DC only
Minimum pulse width	16 nanoseconds
Minimum pulse amplitude	2 Volt
Absolute maximum input	-0.7V to +8V

TRIG OUT Output

Connector Used	AUX I/O
Output Signal	5 Volt TTL
Synchronization	Synchronized to a clock derived from the ADC sampling clock. Divide-by-4 clock (dual channel mode) or divide-by-8 clock (single channel mode)

Materials Supplied

ATS9625 PCI Express Card

ATS9625 Installation Disk (on USB Flash Drive)

Certification and Compliances

CE Compliance

All specifications are subject to change without notice

ORDERING INFORMATION

ATS9625-2G-SL50	ATS9625-002
ATS9625-2G-SE260	ATS9625-003
SyncBoard-9625 2x	ATS9625-007
SyncBoard-9625 4x	ATS9625-008
ATS9625: High Capacity FPGA Upgrade	ATS9625-013
ATS9625: FPGA Development Kit	ATS9625-FDK
C/C++, MATLAB SDK for ATS9625	ATS-SDK
LabVIEW VI for ATS9625	ATS-VI
Linux Driver Source for ATS9625	ATS9625-LIN

Manufactured By:

Alazar Technologies, Inc.

6600 TRANS-CANADA HIGHWAY, SUITE 310
POINTE-CLAIRE, QC, CANADA H9R 4S2

TOLL FREE: 1-877-7-ALAZAR OR 1-877-725-2927
TEL: (514) 426-4899 FAX: (514) 426-2723

E-MAIL: info@alazartech.com