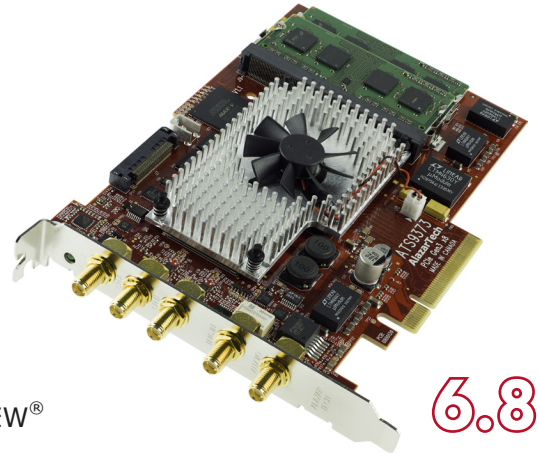
ATS9373

4 GS/s 12-Bit PCIe Gen3 Digitizer

- Up to 4 GS/s 12-bit A/D conversion
- 6.8 GB/s PCIe Gen3 (8-lane) interface
- 2 channel operation at 2 GS/s
- FPGA based FFT processing
- Variable frequency external clocking
- Continuous streaming mode
- ±400 mV fixed input range
- Optional 1.9 GHz wideband upgrade
- AlazarDSO oscilloscope software
- Software Development Kit supports C/C++, C#, Python, MATLAB®, LabVIEW®
- Support for Windows & Linux



RoHS 2 COMPLIANT 2011/65/EU

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6.8 GB/s

Product	Bus	Operating System	Channels	Sampling Rate	Bandwidth	Memory Per Channel	Resolution
ATS9373	PCIe x8 Gen 3	Windows Linux 32-bit/64-bit	2	4 GS/s - 1 ch 2 GS/s - 2 ch	1.0 GHz or Optional 1.9 GHz	4/2 Gigasamples in single/dual channel mode	12 bits

Overview

ATS9373 is an 8-lane PCI Express Gen 3 (PCIe x8), single or dual-channel, high speed, 12 bit, 4 GS/s or 2 GS/s waveform digitizer card capable of acquiring data into its on-board 8GB memory or streaming acquired data to PC memory at rates up to 6.8 GB/s.

It is also possible to do FPGA-based 4096 point FFT on acquired data. This is useful for Optical Coherence Tomography (OCT) related applications.

There are two A/D converters on the ATS9373 board, each running at 2 GS/s. ATS9373 uses interleaved sampling (DES mode) to achieve 4 GS/s sampling.

Optional variable frequency external clock allows operation from 2 GHz down to 500 MHz when using DES mode and from 2 GHz down to 300 MHz when operating in non-DES mode (or 100 MHz for screened ATS9373 cards), making ATS9373 an ideal waveform digitizer for many applications.

Users can capture data from one trigger or a burst of triggers. Users can also stream very large datasets continuously to PC memory or hard disk.

ATS9373 is supplied with AlazarDSO software that lets the user start data acquisition immediately, without having to go through a software development process.

Users who need to integrate the ATS9373 in their own program can purchase a software development kit, ATS-SDK, for C/C++, C#, Python, MATLAB, and LabVIEW for both Windows and Linux operating systems.

All of this advanced functionality is packaged in a low power, half-length PCI Express Gen 3 card.

Applications

Optical Coherence Tomography (OCT)

Ultrasonic & Eddy Current NDT/NDE

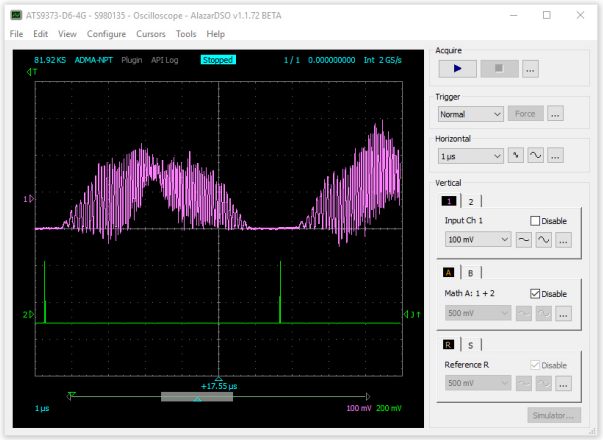
RF Signal Recording & Analysis

Terabyte Storage Oscilloscope

High Resolution Oscilloscope

Spectroscopy

Multi-Channel Transient Recording



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PCI Express Gen 3 Bus Interface
ATS9373 interfaces to the host computer using an 8-lane PCI Express bus. Each lane operates at 8.0 Gbps (Gen 3).

According to PCIe specification, an 8-lane board can be plugged into any 8-lane or 16-lane slot, but not into a 4-lane or 1-lane slot. As such, ATS9373 requires at least one free 8-lane or 16-lane slot on the motherboard.

ATS9373 is fully compatible with motherboards of all generations of PCI Express (Gen 1, Gen 2 or Gen 3). At run-time, ATS9373 and the motherboard negotiate the appropriate link speed and width.

The physical and logical PCIe Gen3 x8 interface is provided by an on-board FPGA, which also integrates acquisition control functions, memory management functions, acquisition datapath and DSP logic. This very high degree of integration maximizes product reliability.

AlazarTech's 6.8 GB/s benchmark was done on an Asus X99 Deluxe motherboard.

Users must always be wary of throughput specifications from manufacturers of waveform digitizers. Some unscrupulous manufacturers tend to specify the raw, burst-mode throughput of the bus. AlazarTech, on the other hand, specifies the benchmarked sustained throughput. To achieve such high throughput, a great deal of proprietary memory management logic and kernel mode drivers have been designed.

Analog Input
An ATS9373 features two analog input channels. Each channel has up to 1.0 GHz of full power analog input bandwidth.

Customers can also order a wideband input upgrade (order number ATS9373-009), which increases the bandwidth to 1.9 GHz in non-DES mode and 1.7 GHz in DES mode.

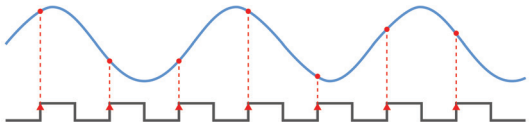
Input voltage range is fixed at ±400 mV.

It must be noted that input impedance of both channels is fixed at 50 Ω. Input coupling is fixed to DC.

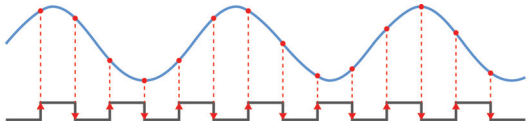
Acquisition System
ATS9373 PCI Express digitizers use state of the art dual 2 GS/s, 12-bit ADCs to digitize the input signals. The two ADCs can be used in dual edge sampling (DES) mode to achieve 4 GS/s sample rate.

If used in dual-channel mode, the two channels are guaranteed to be simultaneous, as the two ADCs use a common clock.

An acquisition can consist of multiple records, with each record being captured as a result of one trigger event. A record can contain both pre-trigger and post-trigger data. Up to 8064 pre-trigger points can be captured in single channel mode and 3968 in dual-channel mode. ATS9373 can capture an infinite number of triggers. In between the multiple triggers being captured, the acquisition system is re-armed by the hardware within 256 sampling clock cycles.



Non-DES Sampling



DES Sampling

This mode of capture, sometimes referred to as Multiple Record, is very useful for capturing data in applications with a very rapid or unpredictable trigger rate. Examples of such applications include medical imaging, ultrasonic testing, OCT and NMR spectroscopy.

On-Board Acquisition Memory
ATS9373 features two DDR3 SODIMM sockets that can each be populated with a 4 GB SODIMM, for a total on-board memory of 8 GB (4 Gigasamples).

This on-board memory is used as a very deep FIFO to temporarily store acquired ADC data before transferring it to motherboard memory using proprietary DMA engines. This on-board buffer allows loss-less data transfer even if the computer is temporarily interrupted by other tasks.

Maximum Sustained Transfer Rate
PCI Express support on different motherboards may vary, resulting in non-optimal data transfer rates. The reasons behind these differences are complex and varied and will not be discussed here.

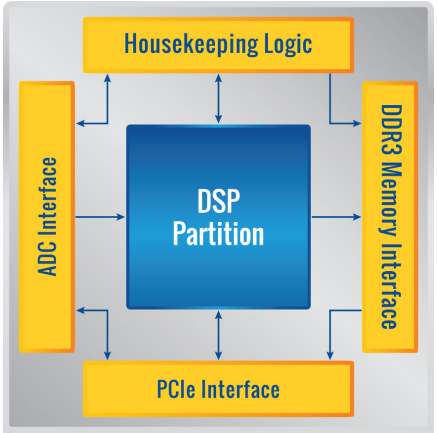
ATS9373 users can quickly determine the maximum sustained transfer rate for their motherboard by inserting their card in a PCIe slot and running the bus benchmarking tool provided in AlazarDSO for Windows or AlazarFrontpanel for Linux software.

Recommended Motherboards or PCs
Many different types of motherboards and PCs have been benchmarked by AlazarTech. The ones that have produced the best throughput results (6.8 GB/s) have been ASUS X99 Deluxe, HP Z440, Z840.

AlazarTech recommends that customers not use SandyBridge CPUs with ATS9373.

FPGA Based Digital Signal Processing

In addition to providing the bus interface and managing the acquisition engine, ATS9373's on-board FPGA is also used for digital signal processing, such as Fast Fourier Transforms.

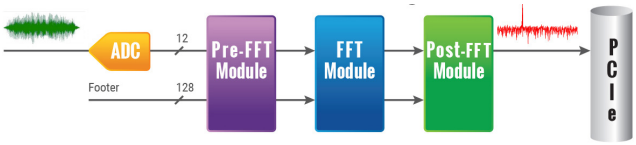


ATS9373 FPGA

ATS9373 is available in two models: ATS9373-A3 (Order number ATS9373-001) features a large Stratix V FPGA 5SGXMA3K3F40C3N, whereas ATS9373-D6 (Order number ATS9373-002) features an even larger and more DSP rich FPGA 5SGSMD6K3F40C3N.

FPGA Based FFT Processing

It is now possible to do real time FFT signal processing using the on-board FPGA. Note that only one input can be processed.



Up to 4096 point FFT length is supported. A user programmable complex windowing function can be applied to the acquired data before FFT calculation.

The complex FFT output is converted to magnitude in single precision floating point format. A logarithmic output is also available.

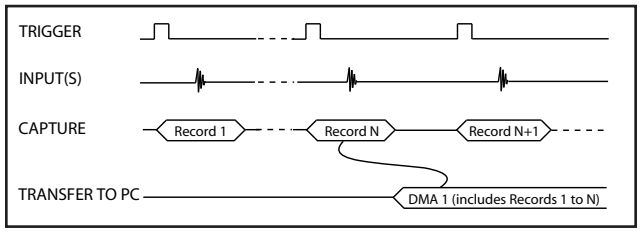
It is also possible to DMA both frequency and time domain data. This allows users to verify FPGA-based FFT operation during algorithm development.

The standard ATS9373-A3 can perform 250,000 4096 point FFTs per second, whereas ATS9373-D6 can do as many as 1,000,000 FFTs per second, i.e. gapless FFT.

No Pre-Trigger (NPT) AutoDMA

Many ultrasonic scanning and medical imaging applications do not need any pre-trigger data: only post-trigger data is sufficient.

NPT AutoDMA is designed specifically for these applications. By only storing post-trigger data, the memory bandwidth is optimized and the entire on-board memory acts like a very deep FIFO.



Note that a DMA is not started until (RecordsPerBuffer +1) number of records (triggers) have been acquired and written to the on-board memory.

NPT AutoDMA buffers do not include headers. However, users can specify that each record should come with its own footer that contains a 40-bit trigger timestamp. The footer is called NPT Footer.

More importantly, a BUFFER_OVERFLOW flag is asserted only if the entire on-board memory is used up. This provides a very substantial improvement over Traditional AutoDMA.

NPT AutoDMA can easily acquire data to PC host memory at the maximum sustained transfer rate of the motherboard without causing an overflow.

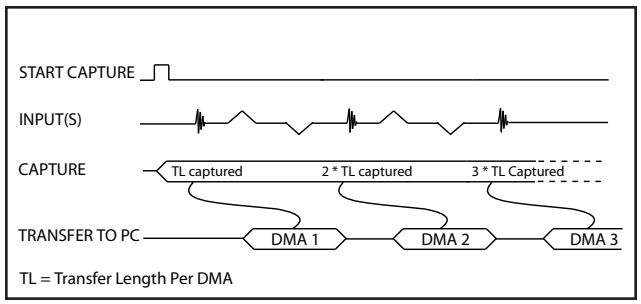
This is the recommended mode of operation for most ultrasonic scanning, OCT and medical imaging applications.

It should be noted that even though this mode is called "No Pre Trigger", it is now possible to do limited pre-trigger data captures, i.e. up to 8192 points in single channel mode and 4096 points in dual channel mode.

Continuous AutoDMA

Continuous AutoDMA is also known as the data streaming mode.

In this mode, data starts streaming across the PCI bus as soon as the ATS9373 is armed for acquisition. It is important to note that triggering is disabled in this mode.



Continuous AutoDMA buffers do not include headers, so it is not possible to get trigger time-stamps. A

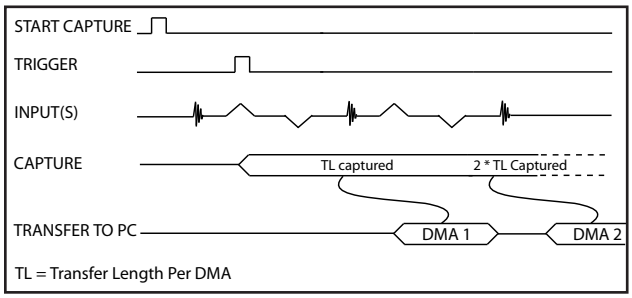
BUFFER_OVERFLOW flag is asserted only if the entire on-board memory is used up.

The amount of data to be captured is controlled by counting the number of buffers acquired. Acquisition is stopped by an AbortCapture command.

Continuous AutoDMA can easily acquire data to PC host memory at the maximum sustained transfer rate of the motherboard without causing an overflow. This is the recommended mode for very long signal recording.

Triggered Streaming AutoDMA

Triggered Streaming AutoDMA is virtually the same as Continuous mode, except the data transfer across the bus is held off until a trigger event has been detected. Triggered Streaming AutoDMA buffers do not include headers, so it is not possible to get trigger time-stamps.



A BUFFER_OVERFLOW flag is asserted only if the entire on-board memory is used up.

As in Continuous mode, the amount of data to be captured is controlled by counting the number of buffers acquired. Acquisition is stopped by an AbortCapture command.

Triggered Streaming AutoDMA can easily acquire data to PC host memory at the maximum sustained transfer rate of the motherboard without causing an overflow. This is the recommended mode for RF signal recording that has to be started at a specific time, e.g. based on a GPS pulse.

Asynchronous DMA Driver

The various AutoDMA schemes discussed above provide hardware support for optimal data transfer. However, a corresponding high performance software mechanism is also required to make sure sustained data transfer can be achieved.

This proprietary software mechanism is called Async DMA (short for Asynchronous DMA).

A number of data buffers are posted by the application software. Once a data buffer is filled, i.e. a DMA has been completed, ATS9373 hardware generates an interrupt, causing an event message to be sent to the application so it can start consuming data. Once the data has been consumed, the application can post the data buffer back on the queue. This can go on indefinitely.

One of the great advantages of Async DMA is that almost 95% of CPU cycles are available for data processing, as all DMA arming is done on an event-driven basis.

To the best of our knowledge, no other supplier of waveform digitizers provides asynchronous software drivers. Their synchronous drivers force the CPU to manage data acquisition, thereby slowing down the overall data acquisition process.

Data Packing Mode

By default, ATS9373 stores 12-bit data acquired by its on-board A/D converters as a 16-bit integer. Users can also choose to pack the data as 12-bit integers or even 8-bit integers. Being able to reduce the total amount of data being transferred can be very useful in data recording applications.

Note that it is the user application's responsibility to unpack the data. Also note that NPT Footers are not available in Data Packing Mode.

Triggering

ATS9373 is equipped with sophisticated digital triggering options, such as programmable trigger thresholds and slope on any of the input channels or the External Trigger input.

While most oscilloscopes offer only one trigger engine, ATS9373 offers two trigger engines (called Engines X and Y).

The user can specify the number of records to capture in an acquisition, the length of each record and the amount of pre-trigger data.

A programmable trigger delay can also be set by the user. This is very useful for capturing the signal of interest in a pulse-echo application, such as ultrasound, radar, lidar etc.

External Trigger Input

ATS9373 external trigger input (TRIG IN) can be set as an analog input with ±2.5 V full scale input range and 50 Ω input impedance, or a 3.3 V TTL input.

When TTL input is selected, the input impedance increases to approximately 6.6 kΩ, making it easier to drive the TRIG IN input from high output impedance sources.

Timebase

ATS9373 timebase can be controlled either by on-board low-jitter VCO or by optional External Clock.

On-board low-jitter VCO uses a 10 MHz TCXO as a reference clock. Clock buffers used feature less than 76 fs_{RMS} additive jitter.

Optional External Clock

While the ATS9373 features low jitter VCO and a 10 MHz TCXO as the source of the timebase system, there may be occasions when digitizing has to be synchronized to an external clock source.

ATS9373 External Clock option provides an SMA input for an external clock signal, which can be a sine wave or square wave signal of minimum 400 mV_{p-p} amplitude. External clock amplitude must not exceed 1.7 V_{p-p}.

Input impedance for the External Clock input is fixed at 50 Ω. External clock input is always ac-coupled.

There are two types of External Clock supported by ATS9373. These are described below.

Fast External Clock

In non-DES mode, a new sample is taken by the on-board ADCs for each rising edge of this External Clock signal.

In DES mode, a new sample is taken on each rising and falling edge of this External Clock signal.

In order to satisfy the clocking requirements of the ADC chips being used, Fast External Clock frequency must always be higher than 300 MHz in non-DES mode (500 MHz in DES mode) and lower than 2 GHz.

For customers whose external clocks may go lower than 300 MHz during the acquisition, it is possible to have AlazarTech screen the ATS9373 boards for external clock operation down to 100 MHz (Order number ATS9373-006)

This is the ideal clocking scheme for OCT applications.

10 MHz Reference Clock

It is possible to generate the sampling clock based on an external 10 MHz reference input. This is useful for RF systems that use a common 10 MHz reference clock.

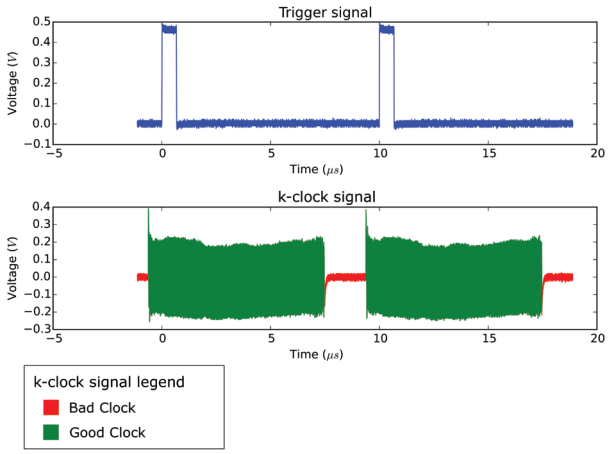
ATS9373 uses an on-board low-jitter PLL to generate a user-specified high frequency clock used by the ADC. This sampling clock can be any multiple of 1 MHz between 300 MHz and 2 GHz.

OCT Ignore Bad Clock

The ADCs used on the ATS9373 require the external clock frequency to be lower than 2 GHz and above 300 MHz (above 500 MHz in DES mode). In OCT applications, these limits cannot always be respected due to the nature of the optical source.

AlazarTech's *OCT Ignore Bad Clock* technology, allows safe operation with these out-of-specification clocks without requiring the use of a dummy clock in the source.

Firmware version 26.04+, driver version 5.10.6+ and SDK 7.1.3+ are required to take advantage of OCT Ignore Bad Clock. For existing customers, these firmware and driver versions are available for download from AlazarTech's website free of charge.



See www.alazartech.com/Technology/OCT-Ignore-Bad-Clock for more information on this technology.

AUX Connector

ATS9373 provides an AUX (Auxiliary) SMA connector that is configured as a Trigger Output connector by default.

When configured as a Trigger Output, AUX SMA connector outputs a 5 Volt TTL signal synchronous to the ATS9373 Trigger signal, allowing users to synchronize their test systems to the ATS9373 Trigger.

When combined with the Trigger Delay feature of the ATS9373, this option is ideal for ultrasonic and other pulse-echo imaging applications.

AUX connector can also be used as a Trigger Enable Input for Frame Capture (B-scan) applications. In fact, this is the most popular use of the AUX connector in OCT applications.

Wideband Input Upgrade

ATS9373 Wideband Input option provides up to 1.9 GHz analog input on two channels (non-DES mode) or up to 1.7 GHz on one channel (DES mode). Input impedance is fixed at 50 Ω.

Calibration

Every ATS9373 digitizer is factory calibrated to NIST- or CNRC-traceable standards. To recalibrate an ATS9373, the digitizer must either be shipped back to the factory or a qualified metrology lab.

On-Board Monitoring

Adding to the reliability offered by ATS9373 are the on-board diagnostic circuits that constantly monitor over 20 different voltages, currents and temperatures. LED alarms are activated if any of the values surpasses the limits.

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AlazarDSO Software
ATS9373 is supplied with the powerful AlazarDSO software that allows the user to setup the acquisition hardware and capture, display and archive the signals.

The Stream-To-Memory command in AlazarDSO allows users to stream a large dataset to motherboard memory.

AlazarDSO software also includes powerful tools for benchmarking the computer bus and disk drive.

Software Development Kits
AlazarTech provides easy to use software development kits for customers who want to integrate the ATS9373 into their own software.

A Windows and Linux compatible software development kit, called ATS-SDK, includes headers, libraries and source code sample programs written in C/C++, C#, Python, MATLAB, and LabVIEW. These programs can fully control the ATS9373 and acquire data in user buffers.

ATS-GPU
ATS-GPU is a software library developed by AlazarTech to allow users to do real-time data transfer from ATS9373 to a GPU card at rates up to 4 GB/s.

Modern GPUs include very powerful processing units and a very high speed graphical memory bus. This combination makes them perfectly suited for signal processing applications.

ATS-GPU-BASE is supplied with an example user application in source code. The application includes GPU kernels that use ATS-GPU to receive data, do very simple signal processing (data inversion), and copy the processed (inverted) data back to a user buffer. All this is done at the highest possible data transfer rate.

Programmers can replace the data inversion code with application-specific signal processing kernels to develop custom applications.

ATS-GPU-OCT is the optional OCT Signal Processing library for ATS-GPU. It contains floating point FFT routines that have also been optimized to provide the maximum number of FFTs per second. Kernel code running on the GPU can do zero-padding, apply a windowing function, do a floating point FFT, calculate the amplitude and convert the result to a log scale. It is also possible to output phase information.

FFTs can be done on triggered data or on continuous gapless stream of data. It is also possible to do spectral averaging. Our benchmarks showed that it was possible to do 1,000,000 FFTs per second when capturing data in single-channel mode and using a NVIDIA GeForce GTX Titan X GPU.

ATS-GPU supports Windows and Linux for CUDA-based development.

Linux Support
AlazarTech offers ATS9373 binary drivers for most of the popular Linux distributions, such as CentOS, Ubuntu,...

Users can download the binary driver for their specific distribution by choosing from the available drivers here:

ftp://release@ftp.alazartech.com/outgoing/linux

Also provided is a GUI application called AlazarFrontPanel that allows simple data acquisition and display.

ATS-SDK includes source code example programs for Linux, which demonstrate how to acquire data programmatically using a C compiler.

If customers want to use ATS9373 in any Linux distribution other than the one listed above, they can have the AlazarTech engineering team generate an appropriate driver for a nominal fee, if applicable.

Based on a minimum annual business commitment, the Linux driver source code license (order number ATS9373-LINUX) may be granted to qualified OEM customers for a fee. For release of driver source code, a Non-Disclosure Agreement must be executed between the customer's organization and AlazarTech.

All such source code disclosures are made on an as-is basis with limited support from the factory.

Export Control Classification
According to the latest Export Control Handbook that came into effect on August 11, 2017, ATS9373 is classified by Export Controls Division of Government of Canada as a controlled product under ECL 1-3.A.2.h, which is equivalent to ECCN 3A002.h.

For sales where the ultimate country destination is Canada or U.S., no export permit is required unless the end-use of ATS9373, in part or in its entirety, is related to the development or deployment of weapons of mass destruction.

For shipments to eligible destinations, AlazarTech is allowed to export under a general export permit, unless the end-use of ATS9373, in part or in its entirety, is related to the development or deployment of weapons of mass destruction. For general export permit shipments, users must provide a signed export compliance statement (ECS) that includes a detailed description of the end-use. Shipments cannot be made without a signed ECS on file.

For all other countries, and for all cases where the end-use of ATS9373, in part or in its entirety, is related to the development or deployment of weapons of mass destruction, an export permit is required, which will require extensive details on the end-use and end-users. This process may cause significant delays.

RoHS Compliance

ATS9373 is fully RoHS compliant, as defined by Directive 2011/65/EU (RoHS 2) of the European Parliament and of the Council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

All manufacturing is done using RoHS-compliant components and lead-free soldering.

EC Conformity

ATS9373 conforms to the following standards:

Electromagnetic Emissions:
CISPR 22:2006/EN 55022:2006 (Class A):
Information Technology Equipment (ITE). Radio disturbance characteristics. Limits and method of measurement.

Electromagnetic Immunity:
CISPR 24:1997/EN 55024:1998 (+A1 +A2):
Information Technology Equipment Immunity characteristics — Limits and methods of measurement.

Safety:
IEC 60950-1:2005: Information technology equipment — Safety — Part 1: General requirements.

IEC 60950-1:2006: Information technology equipment — Safety — Part 1: General requirements.

ATS9373 also follows the provisions of the following directives: 2006/95/EC (Low Voltage Equipment); 2004/108/EC (Electromagnetic Compatibility).

FCC & ICES-003 Compliance

ATS9373 has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15, subpart B of the FCC Rules, and the Canadian Interference-Causing Equipment Standard ICES-003:2004.

ATS9373

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System Requirements

Personal computer with at least one free x8 or x16 PCI Express slot (must be Gen 3 slot to achieve full data throughput), 16 GB RAM, 100 MB of free hard disk space, SVGA display adaptor and monitor with at least a 1024 x 768 resolution.

Power Requirements

+12 V	1.5 A, typical
+3.3 V	3.0 A, typical

Physical

Size	Single slot, half length PCI Express card (4.377 inches x 6.5 inches excluding the connectors protruding from the front panel)
Weight	250 g

I/O Connectors

ECLK, CH A, CH B, TRIG IN, AUX I/O	SMA female connector

Environmental

Operating temperature	0 to 55 degrees Celsius
Storage temperature	-20 to 70 degrees Celsius
Relative humidity	5 to 95%, non-condensing

Acquisition System

Resolution	12 bits
Bandwidth (-3 dB)	
DC-coupled, 50 Ω	Standard DC - 1.0 GHz
Bandwidth with Wideband Upgrade	
Non-DES Mode	DC - 1.9 GHz
DES Mode	DC - 1.7 GHz
Number of channels	2, simultaneously sampled
Maximum Sample Rate	4 GS/s single shot for 1 channel 2 GS/s single shot for 2 channels
Minimum Sample Rate	1 KS/s single shot for internal clocking
Full Scale Input ranges 50 Ω input impedance:	±400 mV
DC accuracy	±2% of full scale in all ranges
Input coupling	DC
Input impedance	50 Ω ±1%
Input protection	
50 Ω	±4 V (DC + peak AC for CH A, CH B and TRIG IN only without external attenuation)

Timebase System

Timebase options	Internal Clock or External Clock (Optional)
Internal Clock accuracy	±2 ppm
Internal Sample Rates	
DES mode:	4 GS/s, 3.6 GS/s, 3 GS/s, 2.4 GS/s
Non-DES mode:	2 GS/s, 1.8 GS/s, 1.5 GS/s, 1.2 GS/s, 1 GS/s, 800 MS/s, 500 MS/s, 200 MS/s, 100 MS/s, 50 MS/s, 20 MS/s, 10 MS/s, 5 MS/s, 2 MS/s, 1 MS/s, 500 KS/s, 200 KS/s, 100 KS/s, 50 KS/s, 20 KS/s, 10 KS/s, 5 KS/s, 2 KS/s, 1 KS/s

Dynamic Parameters

Typical values measured on the 400 mV range of CH A of a randomly selected ATS9373. Input signal was provided by a SRS SG384 signal generator, followed by a 9-pole, 100 MHz band-pass filter (TTE Q36T-100M-10M-50-720BMF). Input frequency was set at 99.9 MHz and output amplitude was set to approximately 95% of the full scale input.

SNR	57.1 dB
SINAD	56.6 dB

Note that these dynamic parameters may vary from one unit to another, with input frequency and with the full scale input range selected.

Optional ECLK (External Clock) Input

Signal Level	400 mVp-p
Input impedance	50 Ω
Input coupling	AC
Maximum frequency	2 GHz for Fast External Clock
Minimum frequency	500 MHz in DES mode 300 MHz in non-DES mode
Minimum frequency for Screened External Clock boards	100 MHz for Fast External Clock
Sampling Edge	Rising and falling in DES mode Rising only in non-DES mode

Optional 10 MHz Reference Input

Signal Level	±200 mV Sine wave or square wave
Input impedance	50 Ω
Input Coupling	AC coupled
Input Frequency	10 MHz ± 0.25 MHz
Sampling Clock Freq.	Any multiple of 1 MHz between: 300 MHz and 2 GHz in non-DES mode 500 MHz and 2 GHz in DES mode

Triggering System

Mode	Edge triggering with hysteresis
Comparator Type	Digital comparators for internal (CH A, CH B) triggering and analog comparators for TRIG IN (External) triggering
Number of Trigger Engines	2
Trigger Engine Combination	OR
Trigger Engine Source	CH A, CH B, EXT, Software or None, independently software selectable for each of the two Trigger Engines
Hysteresis	±5% of full scale input, typical

Trigger sensitivity	±10% of full scale input range. This implies that the trigger system may not trigger reliably if the input has an amplitude less than ±10% of full scale input range selected
Trigger level accuracy	±5%, typical, of full scale input range of the selected trigger source
Bandwidth	250 MHz
Trigger Delay	Software selectable from 0 to 9,999,999 sampling clock cycles
Trigger Timeout	Software selectable with a 10 µs resolution. Maximum settable value is 3,600 seconds. Can also be disabled to wait indefinitely for a trigger event

TRIG IN (External Trigger) Input

Input range	±2.5 V or TTL Input, software selectable
Input impedance	50 Ω for ±2.5 V range 6.6 kΩ ±10% for TTL input
Coupling	DC only
Bandwidth (-3 dB)	DC - 250 MHz
DC accuracy	±10% of full scale input
Input protection	±8 V (DC + peak AC without external attenuation)

TRIG OUT Output

Connector Used	AUX I/O
Output Signal	5 Volt TTL
Synchronization	Synchronized to a clock derived from the ADC sampling clock. Divide-by-4 clock (dual channel mode) or divide-by-8 clock (single channel or DES mode)

Materials Supplied

ATS9373 PCI Express Card

ATS9373 Install Disk on USB flash drive

Certification and Compliances

RoHS 2 (Directive 2011/65/EU) Compliance

CE Marking — EC Conformity

FCC Part 15 Class A / ICES-003 Class A Compliance

All specifications are subject to change without notice

ORDERING INFORMATION

ATS9373-A3	ATS9373-001
ATS9373-D6	ATS9373-002
ATS9373: External Clock Upgrade	ATS9373-005
ATS9373: Screened External Clock Upgrade	ATS9373-006
ATS9373: Wideband Input Upgrade	ATS9373-009
ATS9373-A3: One Year Extended Warranty	ATS9373-061
ATS9373-D6: One Year Extended Warranty	ATS9373-062
Software Development Kit (Supports C/C++, Python, MATLAB, and LabVIEW)	ATS-SDK
ATS-GPU-BASE: GPU Streaming Library	ATSGPU-001
ATS-GPU-OCT: Signal Processing Library (requires ATSGPU-001)	ATSGPU-101

Manufactured By:

Alazar Technologies, Inc.

6600 TRANS-CANADA HIGHWAY, SUITE 310
POINTE-CLAIRE, QC, CANADA H9R 4S2

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TEL: (514) 426-4899 FAX: (514) 426-2723

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DATASHEET REVISION HISTORY

Changes from version 1.6D (Oct 2017) to version 1.6E	Section, Page
Added FFT length	Overview, pg. 1
Added note about NPT Footers	No Pre-Trigger (NPT) AutoDMA, pg. 3
Added note about NPT Footers not being available in Data Packing Mode	Data Packing Mode, pg. 4
Updated external clock minimum amplitude. Correct value is 400 mV_{p-p}	Optional External Clock, pg. 5
Added section on OCT Ignore Bad Clock	OCT Ignore Bad Clock, pg. 5
Added note about Trigger Enable Input use in OCT	AUX Connector, pg. 5
Added CNRC as calibration standard	Calibration, pg. 5
Added -BASE and -OCT to ATS-GPU description for clarity	ATS-GPU, pg. 6
Corrected size of card	Physical, pg. 8
Updated external clock Signal Level. Correct value is 400 mVp-p.	Optional ECLK (External Clock) Input, pg. 8
Updated email address	Manufactured By, pg. 9

Changes from version 1.6C (Sept 2017) to version 1.6D	Section, Page
Updated description for product ATSGPU-001 & ATSGPU-101	Ordering Information System, pg. 8

Changes from version 1.6B (July 2017) to version 1.6C	Section, Page
Specified conditions for obtaining a Linux driver source code license	Linux Support, pg. 6
Added Export Control Classification information	Export Control Classification, pg. 6
Removed product ATS9373-LINUX	Ordering Information System, pg. 8
Added products ATS9373-061 and ATS9373-062	Ordering Information System, pg. 8
Replaced product ATSGPU-1YR with ATSGPU-001	Ordering Information System, pg. 8
Updated description for product ATSGPU-101	Ordering Information System, pg. 8

Changes from version 1.6A (July 2017) to version 1.6B	Section, Page
Added missing Internal Sample Rate in Non-DES mode: 1.8 GS/s	Timebase System, pg. 7

Changes from version 1.6 (July 2016) to version 1.6A	Section, Page
Added note about lower External Clock minimum frequency for cards with Screened External Clock	Overview, pg. 1
Corrected External Trigger input impedance for TTL input	External Trigger Input, pg. 4
Added Screened External Clock to Fast External Clock	Optional External Clock, pg. 5
Added section on Wideband Input	Wideband Input, pg. 5
Modified AlazarDSO description	AlazarDSO Software, pg. 5
Added Python support	Software Development Kit, pg. 5
Modified ATS-GPU description, now supports CUDA-based GPUs	ATS-GPU, pg. 5
Modified Linux Support description	Linux Support, pg. 6
Added section on RoHS Compliance	RoHS Compliance, pg. 6
Added section on EC Conformity	EC Conformity, pg. 6
Added section on FCC & ICES-003 Compliance	FCC & ICES-003 Compliance, pg. 6
Added minimum frequency for Screened External Clock	Optional ECLK (External Clock) Input, pg. 7
Updated External Trigger Input Impedance for TTL input to 6.6 kΩ ±10%	TRIG IN (External Trigger) Input, pg. 8
Updated list of Certification and Compliances	Certification and Compliances, pg. 8
Updated product name for ATS9373-009	Ordering Information, pg. 8
Corrected order number for ATS9373-LINUX	Ordering Information, pg. 8
Removed products ATS9373-007, ATS9373-008	Ordering Information, pg. 8
Added products ATS9373-006, ATSGPU-1YR, ATSGPU-101	Ordering Information, pg. 8