ATS9351

500MS/s 12-Bit PCIe OEM Digitizer

- 1.6 GB/s PCI Express (8-lane) interface
- 2 channels sampled at 12-bit resolution
- 500 MS/s real-time sampling rate
- Variable frequency external clocking
- Up to 2 GigaSample dual-port memory
- Continuous streaming mode
- Low noise ±400mV fixed input range
- Asynchronous DMA device driver
- AlazarDSO oscilloscope software
- Software Development Kits support C/C++, C#, MATLAB and LabVIEW
- Linux driver available

RoHS compliant 2002/95/EC

Product	Bus	Operating System	Channels	Sampling Rate	Bandwidth	Memory Per Channel	Resolution
ATS9351	PCIe x8	Win XP/Vista/7, Linux 2.6+ 32bit/64 bit	2	500 MS/s to 1 KS/s	250 MHz	Up to 2 Gig in single channel mode	12 bits

Overview

ATS9351 is an 8-lane PCI Express (PCIe x8), dual-channel, high speed, 12 bit, 500 MS/s waveform digitizer card capable of streaming acquired data to PC memory at rates up to 1.6 GB/s or storing it in its deep on-board dual-port acquisition memory buffer of up to 2 Gigasamples.

The main difference between ATS9351 and ATS9350 is that ATS9351 has a fixed gain input amplifier that allows analog signals to be captured with a higher signal to noise ratio compared to ATS9350

Target customers for ATS9351 are those who have control over the output amplitude of their sensor and can match it to the full scale input range of ATS9351.

For customers who need variable input gain, we recommend using the ATS9350.

Optional variable frequency external clock allows operation from 500 MHz down to 2 MHz, making ATS9351 an ideal waveform digitizer for OCT applications.

ATS9351 is supplied with AlazarDSO software that lets the user get started immediately without having to go through a software development process.

Users who need to integrate the ATS9351 in their own program can purchase a software development kit, ATS-SDK for C/C++ and MATLAB, or ATS-VI for LabVIEW for Windows or a Linux based ATS-Linux for C/C++ and LabVIEW for Linux.

All of this advanced functionality is packaged in a low power, half-length PCI Express card.

Applications

Optical Coherence Tomography (OCT)

Ultrasonic & Eddy Current NDT/NDE

Radar/RF Signal Recording & Analysis

Terabyte Storage Oscilloscope

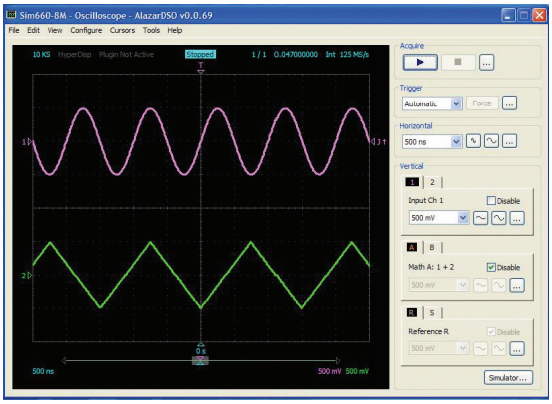
High Resolution Oscilloscope

Lidar

Spectroscopy

Digital Down Conversion (DDC)

Multi-Channel Transient Recording



PCI Express Bus Interface

ATS9351 interfaces to the host computer using an 8-lane PCI Express bus. Each lane operates at 2.5 Gbps. PCIe bus specification v1.0a and v1.1 are supported.

According to PCIe specification, an 8-lane board can be plugged into any 8-lane or 16-lane slot, but not into a 4-lane or 1-lane slot. As such, ATS9351 requires at least one free 8-lane or 16-lane slot on the motherboard.

The physical and logical PCIe x8 interface is provided by an on-board FPGA, which also integrates acquisition control functions, memory management functions and acquisition datapath. This very high degree of integration maximizes product reliability.

PCI Express is a relatively new bus and, as such, throughput performance may vary from motherboard to motherboard. AlazarTech's 1.6 GB/s benchmark was done on an ASUS P6T7 motherboard based on the x58 chipset for iCore processors.

Other motherboards. such as Intel S5000PSL, produced similar results, whereas older machines such as the Dell T7400 also support 1.6 GB/s.

Users must always be wary of throughput specifications from manufacturers of waveform digitizers. Some unscrupulous manufacturers tend to specify the raw, burst-mode throughput of the bus. AlazarTech, on the other hand, specifies the benchmarked sustained throughput. To achieve such high throughput, a great deal of proprietary memory management logic and kernel mode drivers have been designed.

Analog Input

An ATS9351 features two analog input channels. Each channel has up to 250 MHz of full power analog input bandwidth with fixed dc-coupling and ±400mV input range.

The fixed gain analog front-end electronics allows ATS9351 to provide almost 6 dB improvement in signal to noise ratio compared to the ATS9350.

It should be noted that CH A and CH B connectors on ATS9351 are of female SMA type.

Acquisition System

ATS9351 PCI Express digitizers use state of the art 500 MSPS, 12-bit ADCs to digitize the input signals. The real-time sampling rate ranges from 500 MS/s down to 1 KS/s for internal clock and 2 MS/s for external clock.

The two channels are guaranteed to be simultaneous, as the two ADCs use a common clock.

An acquisition can consist of multiple records, with each record being captured as a result of one trigger event. A record can contain both pre-trigger and post-trigger data.

Infinite number of triggers can be captured by ATS9351 when it is operating using dual-port memory.

In between the multiple triggers being captured, the acquisition system is re-armed by the hardware within 256 sampling clock cycles.

This mode of capture, sometimes referred to as Multiple Record, is very useful for capturing data in applications with a very rapid or unpredictable trigger rate. Examples of such applications include medical imaging, ultrasonic testing, OCT and NMR spectroscopy.

On-Board Acquisition Memory

ATS9351 supports on-board memory buffers of 128 Megasamples, 1 Gigasamples and 2 Gigasamples.

Acquisition memory can either be divided equally between the two input channels or devoted entirely to one of the channels.

There are two distinct advantages of having on-board memory:

First, a snapshot of the ADC data can be stored into this acquisition memory at full acquisition speed of 2 ch * 500 MS/s * 2 bytes per sample = 2 Gigabytes per second, which is higher than the maximum PCIe x8 bus throughput of 1.6 GB/s.

Second, and more importantly, on-board memory can also act as a very deep FIFO between the Analog to Digital converters and PCI Express bus, allowing very fast sustained data transfers across the bus, even if the operating system or another motherboard resource temporarily interrupts DMA transfers.

Maximum Sustained Transfer Rate

PCI Express support on different motherboards is not always the same, resulting in significantly different sustained data transfer rates. The reasons behind these differences are complex and varied and will not be discussed here.

ATS9351 users can quickly determine the maximum sustained transfer rate for their motherboard by inserting their card in a PCIe slot and running the Tools:Benchmark:Bus tool provided in AlazarDSO software.

ATS9351, which is equipped with dual-port on-board memory, will be able to achieve this maximum sustained transfer rate.

Recommended Motherboards

Many different types of motherboards have been benchmarked by AlazarTech. The best performance is provided by motherboards that use the Intel x58

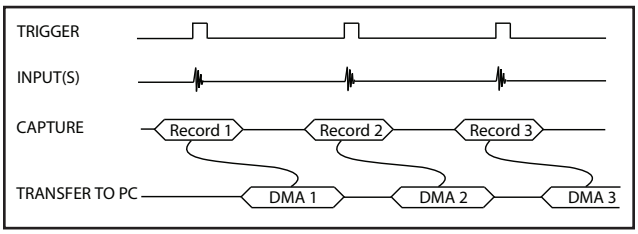
chipset and iCore 7 processors. The motherboard that has consistently given the best throughput results (as high as 1.7 GB/s) has been the ASUS P6T7.

Older motherboards, such as Intel S5000PSLSATA that use the S5000 chipset have also provided very good (1.6 GB/s) sustained throughput.

Many customers have also used workstation class computers from Dell (Precision T3500, T550 & T7500) and HP (Z400, Z600 & Z800) with great success.

Traditional AutoDMA

In order to acquire both pre-trigger and post-trigger data in a dual-ported memory environment, users can use Traditional AutoDMA.



Data is returned to the user in buffers, where each buffer can contain from 1 to 8191 records (triggers). This number is called RecordsPerBuffer.

Users can also specify that each record should come with its own header that contains a 40-bit trigger timestamp.

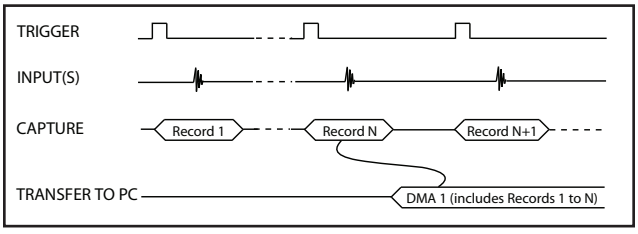
A BUFFER_OVERFLOW flag is asserted if more than 512 buffers have been acquired by the acquisition system, but not transferred to host PC memory by the AutoDMA engine.

In other words, a BUFFER_OVERFLOW can occur if more than 512 triggers occur in very rapid succession, even if all the on-board memory has not been used up.

No Pre-Trigger (NPT) AutoDMA

Many ultrasonic scanning and medical imaging applications do not need any pre-trigger data: only post-trigger data is sufficient.

NPT AutoDMA is designed specifically for these applications. By only storing post-trigger data, the memory bandwidth is optimized and the entire on-board memory acts like a very deep FIFO.



Note that a DMA is not started until RecordsPerBuffer number of records (triggers) have been acquired and written to the on-board memory.

NPT AutoDMA buffers do not include headers, so it is not possible to get trigger time-stamps.

More importantly, a BUFFER_OVERFLOW flag is asserted only if the entire on-board memory is used up. This provides a very substantial improvement over Traditional AutoDMA.

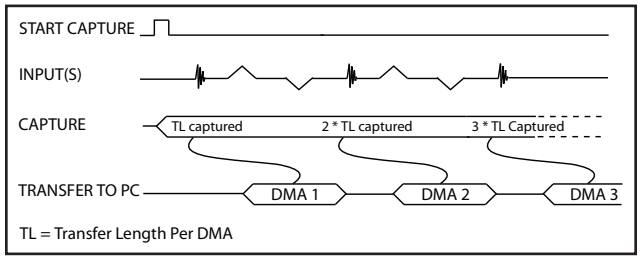
NPT AutoDMA can easily acquire data to PC host memory at the maximum sustained transfer rate of the motherboard without causing an overflow.

This is the recommended mode of operation for most ultrasonic scanning, OCT and medical imaging applications.

Continuous AutoDMA

Continuous AutoDMA is also known as the data streaming mode.

In this mode, data starts streaming across the PCI bus as soon as the ATS9351 is armed for acquisition. It is important to note that triggering is disabled in this mode.



Continuous AutoDMA buffers do not include headers, so it is not possible to get trigger time-stamps.

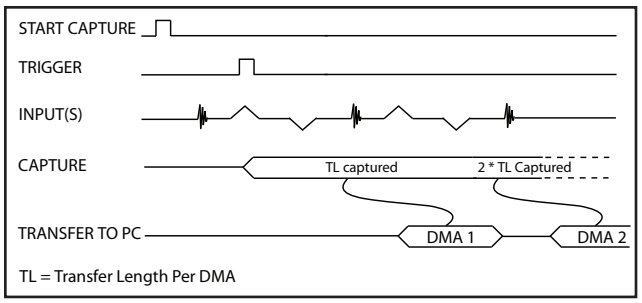
A BUFFER_OVERFLOW flag is asserted only if the entire on-board memory is used up.

The amount of data to be captured is controlled by counting the number of buffers acquired. Acquisition is stopped by an AbortCapture command.

Continuous AutoDMA can easily acquire data to PC host memory at the maximum sustained transfer rate of the motherboard without causing an overflow. This is the recommended mode for very long signal recording.

Triggered Streaming AutoDMA

Triggered Streaming AutoDMA is virtually the same as Continuous mode, except the data transfer across the bus is held off until a trigger event has been detected.



Triggered Streaming AutoDMA buffers do not include headers, so it is not possible to get trigger time-stamps.

A BUFFER_OVERFLOW flag is asserted only if the entire on-board memory is used up.

As in Continuous mode, the amount of data to be captured is controlled by counting the number of buffers acquired. Acquisition is stopped by an AbortCapture command.

Triggered Streaming AutoDMA can easily acquire data to PC host memory at the maximum sustained transfer rate of the motherboard without causing an overflow. This is the recommended mode for RF signal recording that has to be started at a specific time, e.g. based on a GPS pulse.

Disk Storage

When a waveform digitizer generates sustained data throughput at these very high rates, one of the major system-level challenges is to store that data in a disk drive.

If the total data storage requirement is in the 10 GByte range, it is possible to store acquired data in the computer's memory using a RAMDisk. Of course, the host computer must have enough memory installed, but that is becoming easier to do with modern computers.

If total data storage requirement is greater than what can be stored in the host computer's memory, it is essential to build a RAID 0 array using high speed disk drives and one or more hardware RAID controllers. One example of such a RAID-based data storage system is AlazarStream family of products.

Real Time Signal Processing

One of the unique features of AlazarTech's waveform digitizer product line is that acquired data is available for real-time signal processing by the host CPU.

What makes this very powerful is the fact that most modern CPUs have multiple cores, which can be used to do real-time signal processing using parallel processing principles.

If your algorithm can be written to take advantage of parallel processing, this may be a very cost-effective solution for signal processing applications.

AlazarTech has been able to demonstrate that a 2.4 GHz, quad-core CPU can do real-time averaging of acquired data at 1.5 GB/s while using up only 25% of CPU cycles. A faster CPU or a CPU with more cores can do signal processing even faster.

GPU Based Signal Processing

Graphical Processing Units (GPUs) are becoming an increasingly popular method of doing fast signal processing.

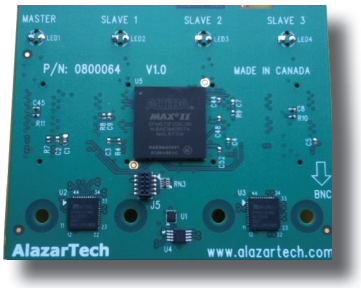
ATS9351 can interface directly to a CUDA-based GPUs using PCI Express bus. Benchmarks using a low cost nVidia GeForce GTX 560 have shown that data can be acquired by ATS9351 and 4096 point FFTs can be calculated by the GPU at sustained rates up to 880MB/s.

This means that users can do real-time 4096 point FFTs on acquired data in single channel mode for trigger repeat rates up to 110 KHz.

Master/Slave Systems

Users can create a multi-board Master/Slave system by synchronizing up to four ATS9351 boards using an appropriate SyncBoard-9351.

SyncBoard-9351 is available as a 2x or a 4x model: the 2x model allows a 2-board Master/Slave system whereas the 4x model allows 2, 3 or 4 board Master/Slave systems.



SyncBoard-9351 is a mezzanine board that connects to the Master/Slave connector along the top edge of the ATS9351 and sits parallel to the motherboard. For additional robustness, users can secure the SyncBoard-9350 to a bracket mounted on each of the ATS9351 boards.

The Master board's clock and trigger signals are copied by the SyncBoard-9351 and supplied to all the Slave boards. This guarantees complete synchronization between the Master board and all Slave boards.

It should be noted that SyncBoard-9351 does not use a PLL-based clock buffer, allowing the use of variable frequency clocks in Master/Slave configuration.

A Master/Slave system samples all inputs simultaneously and also triggers simultaneously on the same clock edge.

Asynchronous DMA Driver

The various AutoDMA schemes discussed above provide hardware support for optimal data transfer. However, a corresponding high performance software mechanism is also required to make sure sustained data transfer can be achieved.

This proprietary software mechanism is called Async DMA (short for Asynchronous DMA).

A number of data buffers are posted by the application software. Once a data buffer is filled, i.e. a DMA has been completed, ATS9351 hardware generates an interrupt, causing an event message to be sent to the application so it can start consuming data. Once the data has been consumed, the application can post the data buffer back on the queue. This can go on indefinitely.

One of the great advantages of Async DMA is that almost 95% of CPU cycles are available for data processing, as all DMA arming is done on an event-driven basis.

To the best of our knowledge, no other supplier of waveform digitizers provides asynchronous software drivers. Their synchronous drivers force the CPU to manage data acquisition, thereby slowing down the overall data acquisition process.

Triggering

ATS9351 is equipped with sophisticated digital triggering options, such as programmable trigger thresholds and slope on any of the input channels or the External Trigger input.

It is also possible to trigger the ATS9351 using a TTL trigger signal with relatively high input impedance of 3 KΩ. This is very useful in imaging applications that use a trigger signal that cannot drive a 50Ω load.

While most oscilloscopes offer only one trigger engine, ATS9351 offers two trigger engines (called Engines X and Y).

The user can specify the number of records to capture in an acquisition, the length of each record and the amount of pre-trigger data.

A programmable trigger delay can also be set by the user. This is very useful for capturing the signal of interest in a pulse-echo application, such as ultrasound, radar, lidar etc.

External Trigger Input

The external trigger input on the ATS9351 is labeled TRIG IN on the face plate.

By default, the input impedance of this input is 50Ω and the full scale input range is +/- 3 Volts. The trigger signal is treated as an analog signal in this situation and a high speed comparator receives the signal.

It is also possible to setup the ATS9351 to trigger off a TTL signal. Input impedance is apprixametly 2 KΩ in this mode.

Timebase

ATS9351 timebase can be controlled either by on-board low-jitter VCO or by optional External Clock.

On-board low-jitter VCO uses an on-board 10 MHz TCXO as a reference clock.

Optional External Clock

While the ATS9351 features low jitter VCO and a 10 MHz TCXO as the source of the timebase system, there may be occasions when digitizing has to be synchronized to an external clock source.

ATS9351 External Clock option provides an SMA input for an external clock signal, which can be a sine wave or LVTTL signal.

Input impedance for the External Clock input is fixed at 50 Ω. External clock input is always ac-coupled.

There are three types of External Clock supported by ATS9351. These are described below.

Fast External Clock

A new sample is taken by the on-board ADCs for each rising edge of this External Clock signal.

In order to satisfy the clocking requirements of the ADC chips being used, Fast External Clock frequency must always be higher than 2 MHz and lower than 500 MHz.

This is the ideal clocking scheme for OCT applications

Slow External Clock

This type of clock should be used when the clock frequency is either too slow or is a burst-type clock. Both these types of clock do not satisfy the minimum clock requirements listed above for Fast External Clock.

In this mode, the ATS9351 ADCs are run at a preset internal clock frequency. The user-supplied Slow External Clock signal is then monitored for low-to-high transitions. Each time there is such a transition, a new sample is stored into the on-board memory.

It should be noted that there can be a 0 to +8 ns sampling jitter when Slow External Clock is being used, as the internal ADC clock is not synchronized to the user-supplied clock.

10 MHz Reference Clock

It is possible to generate the sampling clock based on an external 10 MHz reference input. This is useful for RF systems that use a common 10 MHz reference clock.

ATS9351 uses an on-board low-jitter VCO to generate the 500 MHz high frequency clock used by the ADC. This 500 MHz sampling clock can then be decimated by a factor of 1, 2, 5, 10 or any other integer value that is divisible by 5.

Optional k-Clock Deglitching Firmware

OCT applications require interfacing the ATS9351 to a variable clock frequency (called k-clock) from a swept-source laser.

In some cases, k-clock output from the laser can contain very narrow glitches that do not satisfy FPGA timing and can cause ATS9351 to occasionally mis-trigger.

After many man-years of testing and verification with various lasers, AlazarTech has developed a special firmware for ATS9351 that limits the k-clock signal to a very small portion of the FPGA fabric, thereby eliminating mis-triggering caused by k-clock glitches.

This firmware upgrade is absolutely essential if you are using Axsun 1320nm lasers running at 50 KHz or lower. Many other lasers can also benefit from this firmare upgrade.

Dummy Clock Switchover

ATS9351 has a built-in Dummy Clock generator and a clock switchover mechanism that can be used to avoid operating the A/D chips outside of their specifications when being clocked by a wept source laser.

However, with the advent of k-clock deglitching firmware (see above), most customers have found that they do not need to use Dummy Clock.

Frame Trigger Input

AUX connector can also be used as a Frame Trigger input (also called Trigger Enable Input in AlazarTech literature).

This input allows users to acquire reliable B-Scans in imaging applications.

Calibration

Every ATS9351 digitizer is factory calibrated to NIST-traceable standards. To recalibrate an ATS9351, the digitizer must either be shipped back to the factory or a qualified metrology lab.

On-Board Monitoring

Adding to the reliability offered by ATS9351 are the on-board diagnostic circuits that constantly monitor over 20 different voltages, currents and temperatures. LED alarms are activated if any of the values surpasses the limits.

AlazarDSO Software

ATS9351 is supplied with the powerful AlazarDSO software that allows the user to setup the acquisition hardware and capture, display and archive the signals.

An optional Stream-To-Disk add-on module for AlazarDSO allows users to stream data to hard disk. For the fastest possible streaming, the hard disks have to be used in a RAID 0 configuration.

Users are also able to write their own Plug-In modules. A Plug-In is a DLL that is called each time AlazarDSO receives a data buffer. Many different data processing and control functions can be built into a Plug-In. Examples include Averaging, Co-Adding, controlling acquisition based on an external GPS module etc.

AlazarDSO software also includes powerful tools for benchmarking the computer bus and disk drive.

Software Development Kits

AlazarTech provides easy to use software development kits for customers who want to integrate the ATS9351 into their own software.

A Windows compatible software development kit, ATS-SDK is also offered. It allows programs written in C/C++ and MATLAB to fully control the ATS9351. Sample programs are provided as source code.

A set of high performance VIs for LabVIEW 8.6 and higher, called ATS-VI, can also be purchased.

ATS-Linux

AlazarTech offers ATS9350 binary drivers for CentOS 6.3 x86_64 with kernel 2.6.32-279.5.2.el6.x86_64. These drivers are also 100% compatible with RHEL 6.3.

Also provided is a GUI application called AlazarFrontPanel that allows simple data acquisition and display.

Source code example programs are also provided, which demonstrate how to acquire data programmatically using a C compiler.

If customers want to use ATS9350 in any Linux distribution other than the one listed above, they must purchase a license for Linux driver source code and compile the driver on the target operating system. A Non-Disclosure Agreement must also be executed between the customer's organization and AlazarTech.

All such source code disclosures are made on an as-is basis with limited support from the factory.

ATS9351

500MS/s 12-Bit PCIe OEM Digitizer

System Requirements

Personal computer with at least one free x8 or x16 PCI Express (v1.0a, v1.1 or v2.0) slot, 2 GB RAM, 100 MB of free hard disk space, SVGA display adaptor and monitor with at least a 1024 x 768 resolution.

Power Requirements

+12V	1.2 A, typical
+3.3V	1.1 A, typical

Physical

Size	Single slot, half length PCI Express card (4.2 inches x 6.5 inches excluding the connectors protruding from the front panel)
Weight	250 g

I/O Connectors

CH A, CH B, ECLK	SMA female connector
TRIG IN, AUX I/O	BNC female connectors

Environmental

Operating temperature	0 to 55 degrees Celcius
Storage temperature	-20 to 70 degrees Celcius
Relative humidity	5 to 95%, non-condensing

Acquisition System

Resolution	12 bits
Bandwidth (-3dB)	
DC-coupled, 50Ω	DC - 250 MHz,
Number of channels	2, simultaneously sampled
Maximum Sample Rate	500 MS/s single shot
Minimum Sample Rate	1 KS/s single shot for internal clocking
Full Scale Input range	±400mV
DC accuracy	±2% of full scale in all ranges
Input coupling	DC
Input impedance	50Ω ±1%
Input protection	
CH A, CH B	±1V (DC + peak AC without external attenuation)
TRIG IN	±4V (DC + peak AC without external attenuation)
AUX I/O	-0.7V to +5.5V

Timebase System

Timebase options	Internal Clock or External Clock (Optional)
Internal Sample Rates	500 MS/s, 250 MS/s, 100 MS/s, 50 MS/s, 20 MS/s, 10 MS/s, 5 MS/s, 2 MS/s, 1 MS/s, 500 KS/s, 200 KS/s, 100KS/s, 50 KS/s, 20 KS/s, 10 KS/s, 5 KS/s, 2 KS/s, 1 KS/s
Internal Clock accuracy	±2 ppm

Dynamic Parameters

Typical values measured on CH A of a randomly selected ATS9351. Input signal was provided by a Marconi 2018A signal generator, followed by multi-pole band-pass filters (TTE Q36T family). Inputs were not averaged.

	5 MHz	20 MHz	50 MHz	100 MHz	200 MHz
SNR	61.9 dB	61.41 dB	61.65 dB	61.02 dB	58.75 dB
SINAD	61.17 dB	60.67 dB	59.62 MHz	59.95 dB	55.51 dB
SFDR	75.12 dB	71.27 dB	84.20 dB	81.47 dB	80.61 dB
THD	-69.28 dB	-68.70 dB	-63.91 dB	-66.57 dB	-58.3 dB
ENOB	9.87	9.79	9.61	9.67	8.93

Optional ECLK (External Clock) Input

Signal Level	400mVp-p to 3Vp-p Sine wave or square wave
Input impedance	50Ω
Input coupling	AC
Maximum frequency	500 MHz for Fast External Clock 60 MHz for Slow External Clock
Minimum frequency	2 MHz for Fast External Clock DC for Slow External Clock
Sampling Edge	Rising

Dummy Clock Switchover

Switchover mode	Only when Fast External Clock is selected
Switchover start	Upon end of each record or based on External Trigger input
Switchover time	Programmable with 5 ns resolution

Optional 10 MHz Reference Input

Signal Level	400mVp-p to 3Vp-p Sine wave or square wave
Input impedance	50Ω
Input Coupling	AC coupled
Input Frequency	10 MHz ± 0.25 MHz
Sampling Clock Freq.	500 MHz

Triggering System

Mode	Edge triggering with hysteresis
Comparator Type	Digital comparators for internal (CH A, CHB) triggering and software selectable analog comparators or TTL gate for TRIG IN (External) triggering
Number of Trigger Engines	2
Trigger Engine Combination	OR only
Trigger Engine Source	CH A, CH B, EXT, Software or None, independently software selectable for each of the two Trigger Engines
Hysteresis	±5% of full scale input, typical
Trigger sensitivity	±10% of full scale input range, except for TTL triggering for EXT. This implies that the trigger sys-

	tem may not trigger reliably if the input has an amplitude less than ±10% of full scale input range selected
Trigger level accuracy	±5%, typical, of full scale input range of the selected trigger source
Bandwidth	250 MHz
Trigger Delay	Software selectable from 0 to 9,999,999 sampling clock cycles
Trigger Timeout	Software selectable with a 10 us resolution. Maximum settable value is 3,600 seconds. Can also be disabled to wait indefinitely for a trigger event

TRIG IN (External Trigger) Input

Input type	Analog or TTL, software selectable
Analog Input impedance	50 Ω
Analog Coupling	DC only
Analog Bandwidth (-3dB)	DC - 250 MHz
Analog Input range	±3 V
Analog DC accuracy	±10% of full scale input
Analog Input protection	±4V (DC + peak AC without external attenuation)
TTL Input impedance	3 KΩ
TTL Coupling	DC only
TTL max. frequency	100 MHz MHz
TTL min. pulse amplitude	2 Volts
TTL Input protection	-0.7V to + 5.5V

TRIG OUT Output

Connector Used	AUX I/O
Output Signal	5 Volt TTL
Synchronization	Synchronized to a clock derived from the ADC sampling clock. Divide-by-4 clock (dual channel mode) or divide-by-8 clock (single channel mode)

Materials Supplied

ATS9351 PCI Express Card

ATS9351 Installation Disk (on USB Flash Drive)

Certification and Compliances

CE Compliance, FCC Class A verification

All specifications are subject to change without notice

ORDERING INFORMATION

ATS9351-128M	ATS9351-002
ATS9351-1G	ATS9351-003
ATS9351-2G	ATS9351-004
ATS9351: External Clock Upgrade	ATS9351-005
SyncBoard-9351 2x	ATS9351-007
SyncBoard-9351 4x	ATS9351-008
ATS9351-128M to 1G Upgrade	ATS9351-010
ATS9351-128M to 2G Upgrade	ATS9351-011
ATS9351-1G to 2G Upgrade	ATS9351-012
ATS9351 k-clock Deglitching Firmware	ATS9351-014
C/C++, VB SDK for ATS9351	ATS-SDK
LabVIEW VI for ATS9351	ATS-VI
Linux Driver for ATS9351	ATS9351-LIN

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