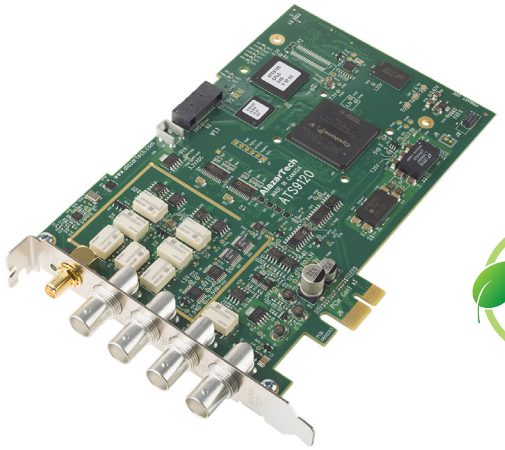
ATS9120
20 MS/s 12-Bit PCIe Digitizer

- 2 channels sampled at 12-bit resolution
- 20 MS/s simultaneous real-time sampling rate on each input
- Continuous streaming mode
- ±40 mV to ±20 V input range
- Asynchronous DMA device driver
- AlazarDSO Oscilloscope Software
- Software Development Kit supports C/C++, C#, Python, MATLAB®, LabVIEW®
- Support for Windows & Linux



RoHS 2 COMPLIANT 2011/65/EU

CE

Product	Bus	Operating System	Channels	Sampling Rate	Bandwidth	Memory Per Channel	Resolution
ATS9120	PCIe x1 Gen 1	32-bit/64-bit Windows & 64-bit Linux	2	20 MS/s to 1 KS/s	10 MHz	Uses on-FPGA FIFO	12 bits

Overview

ATS9120 is a dual-channel, 12 bit, 20 MS/s waveform digitizer card capable of streaming acquired data to motherboard memory. ATS9120 is a single-lane PCI Express (PCIe x1) Gen 1 card, which supports up to 200 MB/s bus throughput.

Users can capture data from one trigger or a burst of triggers. Users can also stream very large datasets continuously to motherboard memory or hard disk.

ATS9120 PCI Express digitizers are an ideal solution for cost sensitive OEM applications that require a digitizer to be embedded into the customer's equipment.

ATS9120 is supplied with AlazarDSO oscilloscope software that lets the user get started immediately without having to write any software.

Users who need to integrate the ATS9120 in their own program can purchase a software development kit, ATS-SDK, for C/C++, C#, Python, MATLAB, and LabVIEW for both Windows and Linux operating system.

All of this advanced functionality is packaged in a low power, half-length PCI Express card.

Applications

Optical Coherence Tomography (OCT)

Ultrasonic & Eddy Current NDT/NDE

Motor Winding Testing

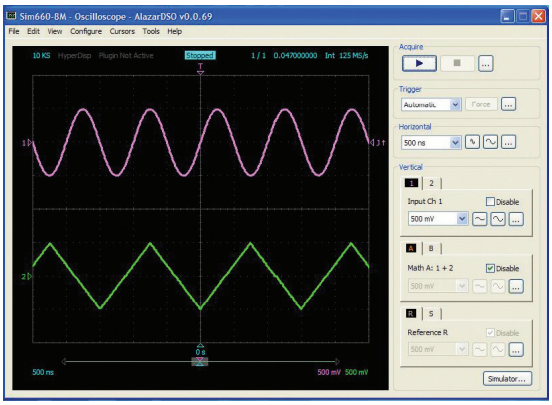
Radar/RF Signal Recording & Analysis

High Resolution Oscilloscope

Lidar

Spectroscopy

Multi-Channel Transient Recording



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PCI Express Bus Interface
ATS9120 interfaces to the host computer using a 1-lane PCI Express bus, operating at 2.5 Gbps.

According to PCIe specification, a 1-lane board can be plugged into any PCIe slot. ATS9120 requires at least one free slot on the motherboard. Electrically, ATS9120 is compatible with Gen 1, Gen 2, and Gen 3 slots.

The physical and logical PCIe x1 interface is provided by an on-board FPGA, which also integrates acquisition control functions, memory management functions and acquisition datapath. This very high degree of integration maximizes product reliability.

AlazarTech's 200 MB/s benchmark was done using an Asus X299-A motherboard.

The same performance can be expected from virtually all other motherboards.

Analog Input
An ATS9120 features two analog input channels with extensive functionality. Each channel has 10 MHz of full power analog input bandwidth. With software selectable attenuation, you can achieve an input voltage range of ±40 mV to ±20 V.

Software selectable AC or DC coupling further increases the signal measurement capability. Software selectable 50 Ω input impedance makes it easy to interface to high speed RF signals.

Acquisition System
ATS9120 PCI digitizers use a pair of 20 MS/s, 12-bit ADCs to digitize the input signals. The real-time sampling rate ranges from 20 MS/s down to 10 KS/s. The two channels are guaranteed to be simultaneous, as they share the exact same clock.

An acquisition can consist of multiple records, with each record being captured as a result of one trigger event. A record may contain up to 4096 points of pre-trigger data.

In between the multiple records being captured, the acquisition system is re-armed by the hardware within 16 sampling clock cycles. This mode of capture, sometimes referred to as Multiple Record, is very useful for capturing data in applications with a very rapid trigger rate.

Examples of such applications include OCT, ultrasonic testing, NMR spectroscopy, motor testing and lightning test.

On-Board Acquisition Memory
ATS9120 uses an on-board FIFO to temporarily store ADC data before DMAing it to motherboard memory.

Since the maximum data rate generated by ATS9120 is only 80 MB/s and its PCIe interface can DMA at 200 MB/s, it is possible to stream a very long, gapless dataset using the on-board FIFO.

FIFO-only acquisition mode can be used for scanning applications such as OCT, ultrasonic inspection, radar and lidar.

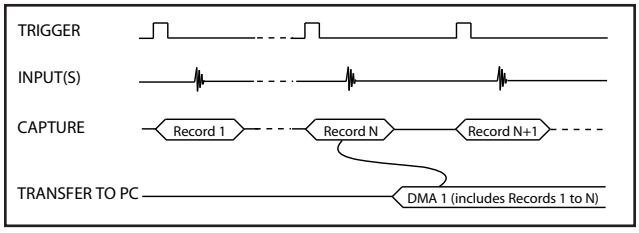
Pre-Trigger Acquisition
It is possible to acquire up to 4096 points of pre-trigger data.

Maximum Sustained Transfer Rate
Virtually all modern motherboards support the specified 200 MB/s throughput.

ATS9120 users can quickly determine the maximum sustained transfer rate for their motherboard by inserting their card in a PCIe slot and running the Tools:Benchmark:Bus tool provided in AlazarDSO software.

No Pre-Trigger (NPT) AutoDMA
Many ultrasonic scanning and medical imaging applications do not need any pre-trigger data: only post-trigger data is sufficient.

NPT AutoDMA is designed specifically for these applications. By only storing post-trigger data, the memory bandwidth is optimized.



Note that a DMA is not started until RecordsPerBuffer number of records (triggers) have been acquired.

NPT AutoDMA buffers do not include headers, so it is not possible to get trigger time-stamps.

More importantly, a BUFFER_OVERFLOW flag is asserted if the FPGA FIFO overflows.

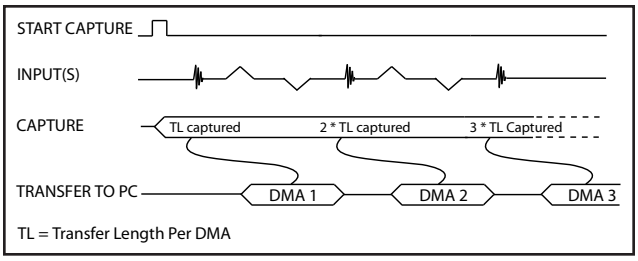
NPT AutoDMA can easily acquire data to PC host memory at the maximum sustained transfer rate of the motherboard without causing an overflow.

This is the recommended mode of operation for most ultrasonic scanning, OCT and medical imaging applications.

It is possible to acquire up to 4096 points of pre-trigger data even in NPT mode.

Continuous AutoDMA
Continuous AutoDMA is also known as the data streaming mode.

In this mode, data starts streaming across the PCI bus as soon as the ATS9120 is armed for acquisition. It is important to note that triggering is disabled in this mode.



Continuous AutoDMA buffers do not include headers, so it is not possible to get trigger time-stamps.

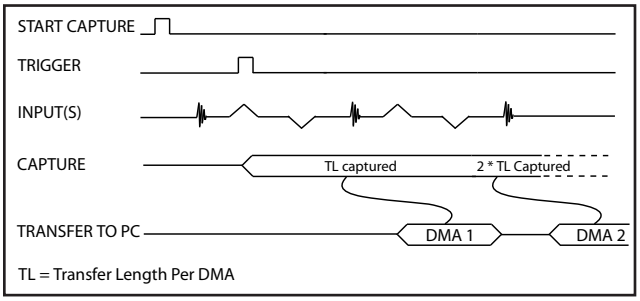
A BUFFER_OVERFLOW flag is asserted if the FPGA FIFO overflows.

The amount of data to be captured is controlled by counting the number of buffers acquired. Acquisition is stopped by an AbortCapture command.

Continuous AutoDMA can easily acquire data to PC host memory at the maximum sustained transfer rate of the motherboard without causing an overflow. This is the recommended mode for very long signal recording.

Triggered Streaming AutoDMA

Triggered Streaming AutoDMA is virtually the same as Continuous mode, except the data transfer across the bus is held off until a trigger event has been detected.



Triggered Streaming AutoDMA buffers do not include headers, so it is not possible to get trigger time-stamps.

A BUFFER_OVERFLOW flag is asserted if the FPGA FIFO overflows.

As in Continuous mode, the amount of data to be captured is controlled by counting the number of buffers acquired. Acquisition is stopped by an AbortCapture command.

Triggered Streaming AutoDMA can easily acquire data to PC host memory at the maximum sustained transfer rate of the motherboard without causing an overflow.

Asynchronous DMA Driver

The various AutoDMA schemes discussed above provide hardware support for optimal data transfer. However, a corresponding high performance software mechanism is also required to make sure sustained data transfer can be achieved.

This proprietary software mechanism is called Async DMA (short for Asynchronous DMA).

A number of data buffers are posted by the application software. Once a data buffer is filled, i.e. a DMA has been completed, ATS9120 hardware generates an interrupt, causing an event message to be sent to the application so it can start consuming data. Once the data has been consumed, the application can post the data buffer back on the queue. This can go on indefinitely.

One of the great advantages of Async DMA is that almost 95% of CPU cycles are available for data processing, as all DMA arming is done on an event-driven basis.

Triggering

The ATS9120 is equipped with sophisticated analog and digital triggering options, such as programmable trigger thresholds and slope on any of the input channels or the External Trigger input.

While most oscilloscopes offer only one trigger engine, ATS9120 offers two trigger engines (called Engines X and Y). This allows the user to combine the two engines using a logical OR operand.

The user can specify the number of records to capture in an acquisition, the length of each record and the amount of pre-trigger data.

A programmable trigger delay can also be set by the user. This is very useful for capturing the signal of interest in a pulse-echo application, such as ultrasound, radar, lidar etc.

External Trigger Input

ATS9120 external trigger input (TRIG IN) can be set as an analog input with ±2.5 V full scale input range and 50 Ω input impedance, or a 3.3 V TTL input.

When TTL input is selected, the input impedance increases to approximately 6 kΩ, making it easier to drive the TRIG IN input from high output impedance sources.

Trigger Time Stamp

A 40-bit time stamp counter comes standard with the ATS9120. By default, this counter is initialized to a zero value when an acquisition session is started and increments once for every sample captured, thus providing a 1-clock timing accuracy. At 20 MS/s sample rate, this counter will not roll over for well over 15 hours.

This allows the user to find out the timing of each trigger in a multiple record acquisition relative to the start of the acquisition.

It is also possible to configure the timestamp counter to reset for the first acquisition only and never again, until a software reset is issued. This feature enables

users to obtain precise timing information about multiple acquisitions.

Optional External Clock

While the ATS9120 features a 10 MHz TCXO as the source of the timebase system, there may be occasions when digitizing has to be synchronized to an external clock source.

ATS9120 External Clock option provides an SMA input for an external clock signal with a frequency between 20 MHz and 1 MHz.

Users can also set a decimation factor for the external clock. For example, if the user wants to digitize the input signal on every tenth clock edge, this factor can be set to 10. Minimum decimation value is 1 and maximum is 100,000.

There are two types of External Clock supported by ATS9120. These are described below.

Fast External Clock

A new sample is taken by the on-board ADCs for each rising (or falling) edge of this External Clock signal.

In order to satisfy the clocking requirements of the ADC chips being used, Fast External Clock frequency must always be higher than 1 MHz and lower than 20 MHz.

10 MHz Reference Clock

It is possible to generate the sampling clock based on an external 10 MHz reference input. This is useful for RF systems that use a common 10 MHz reference clock.

ATS9120 uses an on-FPGA low-jitter PLL to generate the 20 MHz clock used by the ADC.

AUX Connector

ATS9120 provides an AUX (Auxiliary) BNC connector that is configured as a Trigger Output connector by default.

When configured as a Trigger Output, AUX BNC connector outputs a 5 Volt TTL signal synchronous to the ATS9120 Trigger signal, allowing users to synchronize their test systems to the ATS9120 Trigger. Note that the Trigger output is synchronized to a divide-by-8 clock (dual channel mode) or divide-by-16 clock (single channel mode).

When combined with the Trigger Delay feature of the ATS9120, this option is ideal for ultrasonic and other pulse-echo imaging applications.

AUX connector can also be used as a Trigger Enable Input and programmable Clock Output.

Calibration

Every ATS9120 digitizer is factory calibrated for gain and offset accuracy to NIST- or CNRC-traceable standards, using an oscilloscope calibrator. To recalibrate an ATS9120, the digitizer must either be shipped back to the factory or a qualified metrology laboratory.

RoHS Compliance

ATS9120 units are fully RoHS compliant, as defined by Directive 2011/65/EU (RoHS 2) of the European Parliament and of the Council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

All manufacturing is done using RoHS-compliant components and lead-free soldering.

AlazarDSO Software

ATS9120 is supplied with the powerful AlazarDSO software that allows the user to setup the acquisition hardware and capture, display and archive the signals.

The Stream-To-Memory command in AlazarDSO allows users to stream a large dataset to motherboard memory.

AlazarDSO software also includes powerful tools for benchmarking the computer bus and disk drive.

Software Development Kits

AlazarTech provides easy to use software development kits for customers who want to integrate the ATS9120 into their own software.

A Windows and Linux compatible software development kit, called ATS-SDK, includes headers, libraries and source code sample programs written in C/C++, C#, Python, MATLAB, and LabVIEW. These programs can fully control the ATS9120 and acquire data in user buffers.

ATS-GPU

ATS-GPU is a software library developed by AlazarTech to allow users to do real-time data transfer from ATS9120 to a GPU card at full bus speed.

Modern GPUs include very powerful processing units and a very high speed graphical memory bus. This combination makes them perfectly suited for signal processing applications.

ATS-GPU-BASE is supplied with an example user application in source code. The application includes GPU kernels that use ATS-GPU to receive data, do very simple signal processing (data inversion), and copy the processed (inverted) data back to a user buffer. All this is done at the highest possible data transfer rate.

Programmers can replace the data inversion code with application-specific signal processing kernels to develop custom applications.

ATS-GPU-OCT is the optional OCT Signal Processing library for ATS-GPU. It contains floating point FFT routines that have also been optimized to provide the maximum number of FFTs per second. Kernel code running on the GPU can do zero-padding, apply a windowing function, do a floating point FFT, calculate the amplitude and convert the result to a log scale. It is also possible to output phase information.

ATS-GPU supports Windows and Linux for CUDA-based development.

Linux Support

AlazarTech offers ATS9120 binary drivers for most of the popular Linux distributions, such as CentOS, Ubuntu,...

Users can download the binary driver for their specific distribution by choosing from the available drivers here:

ftp://release@ftp.alazartech.com/outgoing/linux

Also provided is a GUI application called AlazarFrontPanel that allows simple data acquisition and display.

ATS-SDK includes source code example programs for Linux, which demonstrate how to acquire data programmatically using a C compiler.

If customers want to use ATS9120 in any Linux distribution other than the one listed above, they can have the AlazarTech engineering team generate an appropriate driver for a nominal fee, if applicable.

Based on a minimum annual business commitment, the Linux driver source code license (order number ATS9120-LINUX) may be granted to qualified OEM customers for a fee. For release of driver source code, a Non-Disclosure Agreement must be executed between the customer's organization and AlazarTech.

All such source code disclosures are made on an as-is basis with limited support from the factory.

Export Control Classification

According to the Export Controls Division of Government of Canada, ATS9120 is currently not controlled for export from Canada. Its export control classification is N8, which is equivalent to ECCN EAR99. ATS9120 can be shipped freely outside of Canada, with the exception of countries listed on the Area Control List and Sanctions List. Furthermore, if the end-use of ATS9120, in part or in its entirety, is related to the development or deployment of weapons of mass destruction, AlazarTech is obliged to apply for an export permit.

EC Conformity

ATS9120 conforms to the following standards:

Electromagnetic Emissions:
CISPR 22:2006/EN 55022:2006 (Class A):
Information Technology Equipment (ITE). Radio disturbance characteristics. Limits and method of measurement.

Electromagnetic Immunity:
CISPR 24:1997/EN 55024:1998 (+A1 +A2):
Information Technology Equipment Immunity characteristics — Limits and methods of measurement.

Safety:
IEC 60950-1:2005: Information technology equipment — Safety — Part 1: General requirements.

IEC 60950-1:2006: Information technology equipment — Safety — Part 1: General requirements.

ATS9120 also follows the provisions of the following directives: 2006/95/EC (Low Voltage Equipment); 2004/108/EC (Electromagnetic Compatibility).

FCC & ICES-003 Compliance

ATS9120 has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15, subpart B of the FCC Rules, and the Canadian Interference-Causing Equipment Standard ICES-003:2004.

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System Requirements

Personal computer with at least one free PCIe slot, 16 GB RAM, 100 MB of free hard disk space, SVGA display adaptor and monitor with at least a 1024 x 768 resolution.

Power Requirements

+12 V	1 A, typical
+3.3 V	0.25 A, typical

Physical

Size	Single slot, half length PCI Express card (4.377 inches x 6.5 inches excluding the connectors protruding from the front panel)
Weight	142 g

I/O Connectors

CH A, CH B, TRIG IN, AUX I/O	BNC female connectors
ECLK	SMA female connector

Environmental

Operating temperature	0 to 55 degrees Celsius
Storage temperature	-20 to 70 degrees Celsius
Relative humidity	5 to 95%, non-condensing

Acquisition System

Resolution	12 bits Data is returned as MSB-justified 16 bit unsigned integers
Bandwidth (-3 dB)	
DC-coupled, 1 MΩ	DC - 10 MHz
DC-coupled, 50 Ω	DC - 10 MHz
AC-coupled, 1 MΩ	10 Hz - 10 MHz
AC-coupled, 50 Ω	100 kHz - 10 MHz
Bandwidth flatness:	± 3 dB
Number of channels	2, simultaneously sampled
Maximum Sample Rate	20 MS/s single shot
Minimum Sample Rate	1 KS/s single shot for internal clocking
Full Scale Input ranges	
1 MΩ input impedance:	±40 mV, ±50 mV, ±80 mV, ±100 mV, ±200 mV, ±400 mV, ±500 mV, ±800 mV, ±1 V, ±2 V, ±4 V, ±5 V, ±8 V, and ±10 V, software selectable
50 Ω input impedance:	±40 mV, ±50 mV, ±80 mV, ±100 mV, ±200 mV, ±400 mV, ±500 mV, ±800 mV, ±1 V, ±2 V, and ±4 V, software selectable
DC accuracy	±2% of full scale in all input ranges
Input coupling	AC or DC, software selectable
Input impedance	50 Ω or 1 MΩ ±1% in parallel with 55 pF ±5 pF, software selectable For input ranges ≥2 V: 53 pF ±2 pF For input ranges ≤1 V: 56 pF ±2 pF
Input protection	
1 MΩ	±28 V (DC + peak AC for CH A, CH B and EXT only without external attenuation)
50 Ω	±4 V (DC + peak AC for CH A, CH B and EXT only without external attenuation)

On-Board Acquisition Memory System

Onboard acq memory	On-FPGA FIFO
Record Length	Software selectable, specified in number of sample points. Must be a minimum of 256 points and must be a multiple of 16.
Number of Records	Software selectable from a minimum of 1 to a maximum of infinite number of records
Pre-trigger depth	
Single-channel	0 to 4080, software selectable with 16 point resolution
Dual-channel	0 to 2040, software selectable with 16 point resolution
Post-trigger depth	Record Length - Pre-trigger depth

Timebase System

Timebase options	Internal Clock or External Clock (Optional)
Internal Sample Rates	20 MS/s, 10 MS/s, 5 MS/s, 2 MS/s, 1 MS/s, 500 KS/s, 200 KS/s, 100 KS/s, 50 KS/s, 20 KS/s, 10 KS/s, 5 KS/s, 2 KS/s, 1 KS/s
Internal Clock accuracy	±25 ppm

Dynamic Parameters

Typical values measured using a randomly selected ATS9120 in ±1 V input range, DC coupling and 50 Ω impedance. Input was provided by a HP8656A signal generator, followed by a 9-pole, 1 MHz band-pass filter. Input frequency was set at 1 MHz and amplitude was 650 mV rms (92% of full scale input).

SNR	60 dB
SINAD	58 dB
THD	-61 dB
SFDR	-62 dB

Note that these dynamic parameters may vary from one unit to another, with input frequency and with the full scale input range selected.

Optional ECLK (External Clock) Input

Signal Level	±200 mV sine wave or 3.3 V LVTTL
Input impedance	50 Ω for AC signals 10 kΩ for DC
Input coupling	AC
Maximum frequency	20 MHz for Fast External Clock
Minimum frequency	1 MHz for Fast External Clock
Sampling Edge	Rising
Maximum amplitude	2 V_{p-p}

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Optional 10 MHz Reference Input

Signal Level	±200 mV sine wave or square wave
Input impedance	50 Ω
Input Coupling	AC coupled
Input Frequency	10 MHz ± 0.25 MHz
Sampling Clock Freq.	20 MHz fixed. Lower sample rates available using decimation

Triggering System

Mode	Edge triggering with hysteresis
Comparator Type	Analog comparators
Number of Trigger Engines	2
Trigger Engine Combination	Engine J, engine K, J OR K, software selectable
Trigger Engine Source	CH A, CH B, EXT, Software or None, independently software selectable for each of the two Trigger Engines
Hysteresis	±5% of full scale input, typical
Trigger sensitivity	±10% of full scale input range. This implies that the trigger system may not trigger reliably if the input has an amplitude less than ±10% of full scale input range selected
Trigger level accuracy	±5%, typical, of full scale input range of the selected trigger source
Bandwidth	10 MHz
Trigger Delay	Software selectable from 0 to 9,999,999 sampling clock cycles. Has to meet alignment requirements (see ATS-SDK User Manual for more information).
Trigger Timeout	Software selectable with a 10 µs resolution. Maximum settable value is 3,600 seconds. Can also be disabled to wait indefinitely for a trigger event

TRIG IN (External Trigger) Input

Input impedance	
±2.5 V range	1 MΩ
TTL range	10 kΩ
Bandwidth (-3 dB)	
DC-coupled	DC - 10 MHz
AC-coupled	10 Hz - 10 MHz
Input range	±2.5 V or TTL, software selectable
DC accuracy	±10% of full scale input
Input protection	±8 V (DC + peak AC without external attenuation)
Coupling	DC, fixed

Materials Supplied

ATS9120 PCIe Card

ATS9120 Installation Disk (on USB Flash Drive)

ORDERING INFORMATION

ATS9120	ATS9120-001
ATS9120: External Clock Upgrade	ATS9120-005
ATS9120: One Year Extended Warranty	ATS9120-061
Software Development Kit (Supports C/C++, Python, MATLAB, and LabVIEW)	ATS-SDK
ATS-GPU-BASE: GPU Streaming Library	ATSGPU-001
ATS-GPU-OCT: Signal Processing Library (requires ATSGPU-001)	ATSGPU-101

Certification and Compliances

RoHS 2 (Directive 2011/65/EU) Compliance

CE Marking — EC Conformity

FCC Part 15 Class A / ICES-003 Class A Compliance

All specifications are subject to change without notice

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